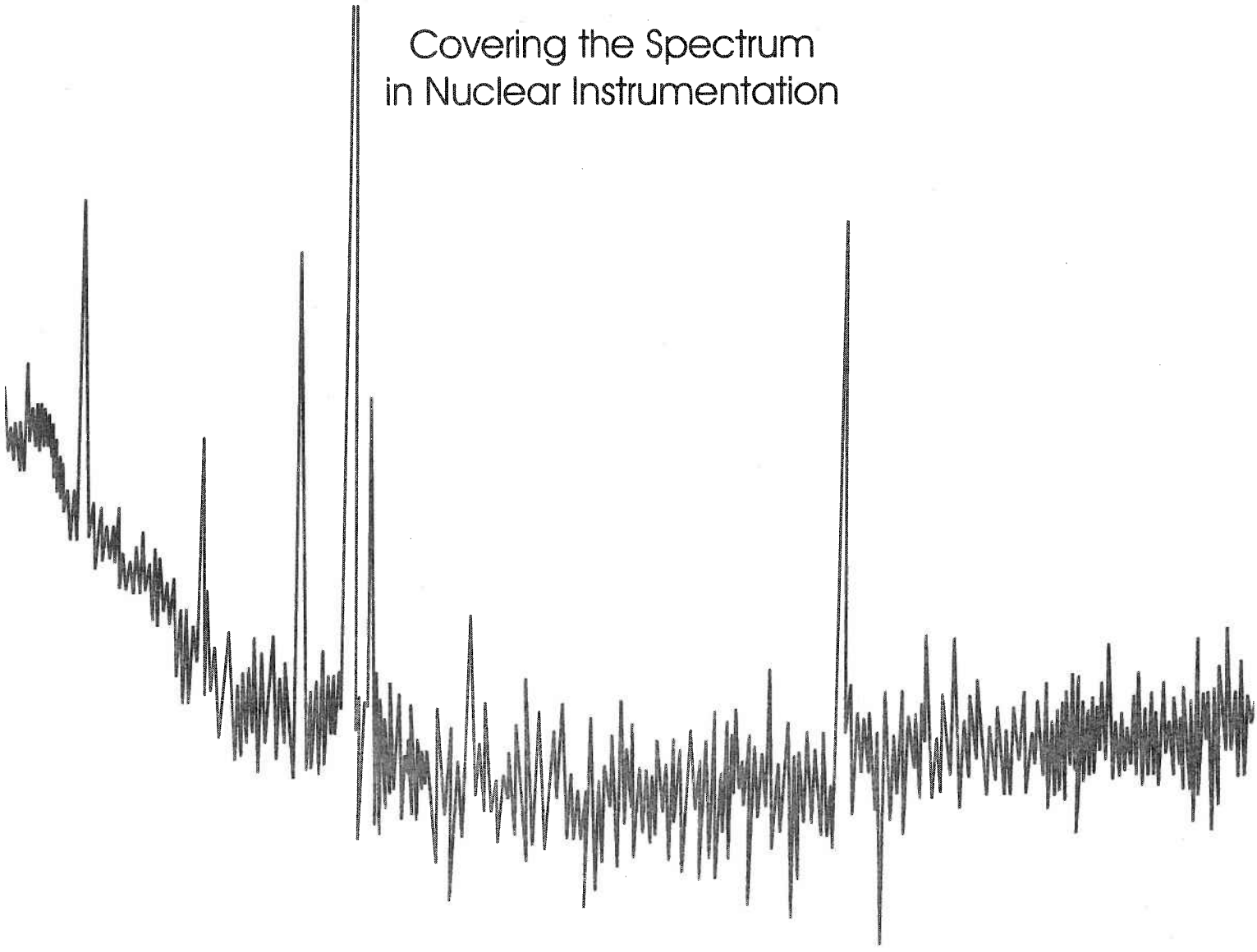
CANBERRA

SERIES 40
MULTICHANNEL ANALYZER

Operator's Manual
Revised July, 1983

Covering the Spectrum
in Nuclear Instrumentation



SERIES 40
MULTICHANNEL ANALYZER

Operator's Manual
Revised July, 1983

Canberra Industries, Inc., One State Street, Meriden, CT 06450 Tel. (203) 238-2351 TWX: 710-461-0192 Cable: CANBERRA

M152R1 8/83 Printed in U.S.A.

Addition
to the Series 40 Operator's Manual

Appendix A.1:
Add -

For domestic operation at 220 volts, the supplied power cord should be replaced with a Underwriters' Laboratories listed, 220 volt-compatible power cord, such as Belden's part number 17566.

Change Table A.1 -

100/120 V fuse rating from 2 A slow-blow to 1.5 A slow-blow.
200/240 V fuse rating from 1 A slow-blow to 0.75 A slow-blow.

Table of Contents

		Page
1.	**INTRODUCTION**	
1.1	General Description	1
1.2	Applications	2
2.	**BASIC SERIES 40 OPERATION**	
2.1	Power On	5
2.2	System Initialization	5
2.3	Basic Dialogue Procedures	5
2.4	LED Indicators	6
2.5	Signal Connectors	6
2.6	Gate	7
2.7	Sampled Voltage Analysis	7
2.8	Positive/Negative Inputs	7
2.9	Sampled Voltage Analysis	7
2.10	Dead Time	7
3.	**USING PHA and MCS**	
3.1	Setups	8
3.2	Data Acquisition	8
3.3	Data Manipulation	9
3.4	MCS Mode	10
4.	**FRONT PANEL FUNCTIONS**	
4.1	Vertical Range and X2 Gain	11
4.2	Mixer/Router	12
4.3	Memory	12
4.4	ADC Gain	12
4.5	ADC Offset	12
4.6	Zero	12
4.7	Add and Subtract	12
4.8	PHA	13
4.9	MCSS	13
4.10	MCSR	13
4.11	LLD (Lower Level Discriminator)	13
4.12	ULD (Upper Level Discriminator)	13
4.13	Amplifier Gain	13
4.14	Clear Time and Clear Data	13
4.15	Read In and Read Out	13
4.16	Collect	13
5.	**KEYBOARD FUNCTIONS**	
5.1	Keypad	14
5.2	Control	14
5.3	Overlap	14
5.4	Transfer	15
5.5	Preset	15
5.6	Region of Interest	15
5.7	Expand Mode	16
5.8	Roll	16
5.9	Integral	16
5.10	Cursor Control	16
5.11	Index	16
5.12	Home	17
5.13	Energy Calibrate	17
5.14	Strip	18
5.15	Spectrum Normalization	18
5.16	Ratio Computation	18
5.17	Area	19

		Page
6.	**INPUT/OUTPUT**	
6.1	Data Readout	19
6.2	Cassette Recorder I/O	20
6.3	Playback of Data	20
6.4	Teletype I/O	20
6.5	Alphanumeric Data ID	20
6.6	Recycle	21
6.7	Model 4251 X-Y Plotter	21
6.8	Model 4253 Graphics Plotter	23
7.	**ANALYSIS OPTIONS**	
7.1	Model 4241 Define/Use	25
7.2	Model 4242 Learn/Execute	32
8.	**WIRING OPTIONS**	
8.1	Model 4231A Mixer/Router Wiring	34
8.2	Model 4232 External Control Wiring	34
8.3	Model 4233 Digital Stabilizer Wiring	36
8.4	Model 4234 Pile-Up Rejection Live Time Correction Wiring	36
9.	**SIGNAL PROCESSING OPTIONS**	
9.1	Model 4221 Amplifier/ADC	37
9.2	Model 4222 High-Performance MCS	37
9.3	Model 4223 Multi-ADC Interface	37
APPENDIX A.		
Internal Controls and Connector Signals		
A.1	Operating Voltage Selection	39
A.2	CPU Board	40
A.3	ADC Board	40
A.4	Display Board and Monitor	40
A.5	Miscellaneous Logic Board	40
A.6	Low Voltage Power Supply	42
A.7	X-Y Plotter Board	43
A.8	Serial Interface Board	43
A.9	Mag Tape Interface Board	43
A.10	GPIB Interface Board	44
A.11	Rear Panel Connectors	44
APPENDIX B.		
Field Installation Instructions		
B.1	Introduction	50
B.2	Model 4222 High-Performance MCS Option	54
B.3	Model 4223 Multi-ADC Interface	54
B.4	Model 4231A Mixer/Router Wiring	55
B.5	Model 4232 External Control Wiring	55
B.6	Model 4233 Digital Stabilizer Wiring	56
B.7	Model 4234 PUR/LTC Wiring	57
B.8	Models 4241 Define Use/AP-PAK and 4242 Learn/Execute Options	57
	Model 4251 X-Y Plotter Interface	59
B.10	Model 4252 Printer Plotter Interface	59
B.11	4253 Graphics Plotter Interface	59
B.12	Model 4254 Magnetic Tape Interface	61
B.13	Model 4271 Computer Interface	62
B.14	Model 4272 GPIB Interface	63
B.15	Models 4273, 4273A, 4273B Computer Interfaces	64

Page

APPENDIX C.
ADC Zero Adjustment Methods
C.1 Energy Calibrate Method 65
C.2 Live Source Method 65
C.3 Pulser Method 65

APPENDIX D.
Computational Methods
D.1 Computations 66

APPENDIX E.
Input/Output Formats
E.1 Series 40 ASCII Mode of I/O 66
E.2 Series 40 Binary Mode of I/O 67

APPENDIX F.
AP-PAK Equations
F.1 Examples 67

APPENDIX G.
Firmware/Option Compatibility
G.1 Options and Successive Versions 68

GLOSSARY OF TERMS 70

FIGURE LISTING

Page

Figure 1-1 Series 40 Block Diagram 1
Figure 1-2 PHA Operation 2
Figure 1-2a Input Voltage Pulses 2
Figure 1-2b PHA Histogram 2
Figure 1-3 Pulse Train Conversion to a PHA Histogram 3
Figure 1-3a Voltage Train Output from NaI Detector 3
Figure 1-3b Resultant Series 40 PHA Histogram 3
Figure 1-4 Effect of 8192 Conversion Gain and 4096 Channel Memory 3
Figure 1-5 Multichannel Scaling 4
Figure 1-5a Input Pulse Train 4
Figure 1-5b MCS Histogram 4
Figure 2-1 Initial Display 5
Figure 2-2 Signal Connectors 6
Figure 2-3 Typical PHA Spectrum (NaI detector) showing Dead Time Bar Graph 7
Figure 3-1 Charge Sensitive System Setup 8
Figure 3-2a Voltage Sensitive System Setup (NaI) 8
Figure 3-2b Voltage Sensitive System Setup [Ge(Li)] 8
Figure 3-3 Transfer Dialogue and Display 9
Figure 3-4 NaI Spectrum with 3 ROI's Entered 9
Figure 3-5 An Expanded ROI 9
Figure 3-6 An ROI with AREA Enabled 9
Figure 3-7 Strip Dialogue and Display 10
Figure 3-8 Clear Time Performed, Channel 0 has Zero Counts 10
Figure 3-9 Typical MCSR Spectrum after 187 251 Sweeps 11
Figure 3-10 X2 Enabled 11
Figure 4-1 Front Panel 11

Page

Figure 5-1 Keyboard Layout 14
Figure 5-2 Initial Energy Calibrate 17
Figure 5-3 Lower Energy Peak Entered 17
Figure 5-4 High Energy Peak Entered 17
Figure 5-5 First ROI's Limits as Energy Units 17
Figure 6-1 Full Memory Readout 21
Figure 6-2 ROI BRIEF Readout 21
Figure 6-3 Energy Calibrated Readout 21
Figure 6-4 Typical X-Y Plot 22
Figure 6-5 Typical Graphics Plot 24
Figure 7-1 Readout Showing Define/Use Equation 26
Figure 7-2 Define Enabled 28
Figure 7-3 Yes Reveals Choice of Define or Load 28
Figure 7-4 Yes Reveals the X Register 29
Figure 7-5 % ERR Equation Entered in X Register 29
Figure 7-6 STORE Places the Equation in Memory 29
Figure 7-7 Dialogue for Entering Constants 29
Figure 7-8 Variable Dialogue 29
Figure 7-9 Second Variable 29
Figure 7-10 Save Dialogue 30
Figure 7-11 Define Pressed to Enter Equation #2 30
Figure 7-12 Variable 1 Entered as Counts 30
Figure 7-13 Variable 2 Entered as Counts 30
Figure 7-14 Equation 2 Completed. USE Enabled 30
Figure 7-15 Store Pressed. Enabling the Accumulator 30
Figure 7-16 Further Data Acquired 31
Figure 8-1 System Interconnection 34
Figure 8-3 Stabilizer Timing Diagram 36
Figure 8-4 System Interconnection 36
Figure 9-1 PHA Cycle Timing Diagram 38
Figure 9-2 Model 4223 Interface Jumpers 39
Figure A-1 J4. Line Voltage Selection Card 40
Figure A-2 CPU Board 41
Figure A-3a Early ADC Board 41
Figure A-3b Revision G ADC Board 41
Figure A-4 Miscellaneous Logic Board 42
Figure A-4 Miscellaneous Logic Board 42
Figure A-5 Mag Tape Interface Board 44
Figure A-6 X-Y Plotter Interface Board 45
Figure A-7 Serial Interface Board 45
Figure A-8 Series 40 Rear Panel 46
Figure B-1 Series 40 Board Locations 50
Figure B-2 Series 40 Rear Panel 51
Figure B-3 Mother Board - Bottom View 51
Figure B-4 CPU Board 52
Figure B-5 Display Board 53
Figure B-6 Display at Power On 53
Figure B-7 Connector Orientation 54
Figure B-8 Miscellaneous Logic Board 54
Figure B-9 Model 8200-PC1 56
Figure B-10a Early ADC Board 58
Figure 8-10b Revision G ADC Board 58
Figure B-11 Model 4252 Printer/Plotter Interface Board 60
Figure B-12 Magnetic Tape Interface Board 61
Figure B-13 Model 4271 Computer Interface Board 64
Figure B-14 Model 4272 GPIB Interface Board 64
Figure D-1 Net Area 66
Figure E-1 Sample ROI Readout from Series 40 ASCII Mode 67

PREFACE

The Series 40 Operator's Manual is organized so that it can be used by both the experienced MCA operator and the newcomer to nuclear analysis. It is divided into several sections for ease of reference:

1. An introduction to the Series 40 Multichannel Analyzer and a basic description of the two modes of operation—PHA and MCS.
2. Basic operating rules for the Series 40.
3. Two simple experiments to show how to use the PHA mode and the MCS mode.
4. A description of the Front Panel functions.
5. A description of the Keyboard functions.
6. A section dealing with the input and output of data.
7. A section covering the Analysis Options.
8. A section on the Wiring Options.
9. A section concerning the Signal Processing Options.

The experienced MCA operator may wish to proceed directly to sections 2, 4, and 5 to learn the specific functions of the Series 40 MCA. The less experienced operator should study the first sections before attempting more than the most basic use of the analyzer. Sections 4 through 8 assume a working knowledge of sections 1,2 and 3.

CLEANING THE FAN FILTER

The fan filter at the rear of the Series 40 must be cleaned periodically (every month or so, depending on the environment) to assure a flow of cooling air to the interior of the analyzer.

If the internal temperature of the Series 40 analyzer is allowed to rise above a safe level, a thermal cutout will remove power from the analyzer to allow the temperature to go down. This will, of course, cause data to be lost unless the Model 8681 Standby Power Supply is connected to the analyzer.

To clean the filter, pull it out of the fan mount. After thoroughly cleaning the filter, replace it inside the fan mount so that the filter completely covers the fan's air intake opening.

The filter may be cleaned by brushing, by blowing with compressed air or by washing. If the filter is washed, be certain that it is completely dry before replacing it in the analyzer.

CLEANING THE MONITOR

A high-voltage induced static charge on the face of the display monitor can attract dust. To remove the dust, clean the face of the monitor with a soft cloth dampened with water. Note that the area being cleaned is a plastic anti-glare filter; take care not to scratch it.

To avoid further static charge accumulation while wiping the screen, hold on to the frame of the Series 40 while cleaning the display.

Section 1. Introduction

1.1 General Description

Functionally, the Series 40 consists of a master controller and five sections: memory, display, signal processing, operator/MCA interface, and data input/output. The controller is a microprocessor which reads its instructions from a permanent program in the memory which controls the MCA functions and directs the use of the 4200 bus. See Figure 1-1.

The memory consists of the preprogrammed Read Only Memory (ROM), which contains the instructions for the microprocessor (firmware), and the Random Access Memory (RAM), which stores operator instruction and the acquired data.

The Series 40 is offered with data memory of 1024, 4096 or 8192 channels. Memory storage in RAM can take place in the full memory, either half of the memory or any quarter of the memory as selected by the operator. Data storage may be either in the Pulse Height Analysis (PHA) mode, the Sampled Voltage Analysis (SVA) mode, or the Multichannel Scaling (MCS) mode. For both PHA and MCS, the data may be added to or subtracted from the memory.

The display section of the Series 40 directs the data in the memory to the large screen display and organizes it in a readily understood format. The operator is supplied with a clear picture of the spectral data in memory and with appropriate information in alphanumeric form as an aid in interpreting the data displayed.

The signal processing section includes a preamplifier/amplifier that may be configured by the operator to accept either charge-sensitive input signals or voltage-sensitive input signals, depending on the type of detector to be used. The signals are passed to an Analog-to-Digital Converter (ADC), which converts the input linear signals to digital form and routes them to the appropriate memory location for storage and subsequent display, analysis and readout.

The operator/MCA interface allows the operator to direct the tasks of the MCA by means of the settings of the control switches on the Control Panel and the pushbuttons on both the Control Panel and the Keyboard. The operator's instructions are routed through the keyboard interface to the RAM section of the memory by way of the microprocessor and the 4200 bus.

The input/output (I/O) section controls the data flow between the RAM section of the memory and the various peripheral devices. As a standard feature, this section includes the I/O interfacing needed to handle current-loop (Teletype) and either EIA RS232 devices or the Canberra Model 5411 Digital Cassette Recorder.

Provision is made for the operator to read prerecorded data into the memory as well as reading data out of the memory in the operator's choice of: full, half or quarter memory; any Regions of Interest, as specified by the operator.

By dividing the MCA's full range of operating features and analysis functions between several sections controlled by a high-speed microprocessor, the Series 40 has been made into an instrument that is well suited to both basic and advanced nuclear analysis needs.

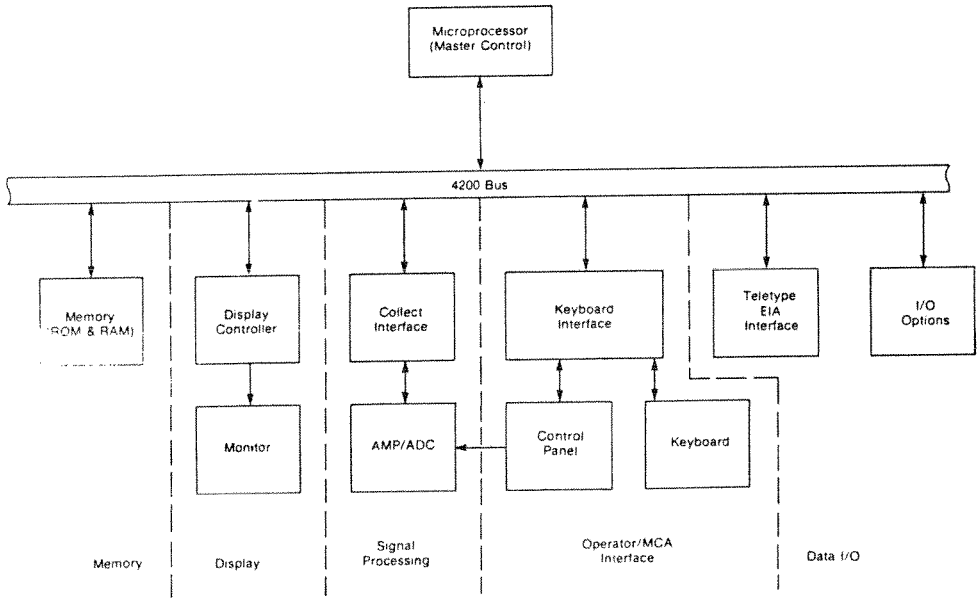


Figure 1-1
Series 40 Block Diagram

1.2 Applications

From a data acquisition point of view, all Series 40 Multichannel Analyzer applications can be placed into one of two categories: Pulse Height Analysis (PHA) or Multichannel Scaling (MCS). These two analysis modes and their applications are discussed in the following sections.

1.2.1 Pulse Height Analysis

In the PHA operating mode, a train of pulses, such as those from a radiation detector, are applied to the input of the Series 40. These pulses have amplitudes (heights) which are proportional to the energies of the incident radiation that was absorbed by the detector. By counting the number of occurrences of pulses of each height and forming a histogram, the Series 40 records the radiation energy spectrum as seen by the detector.

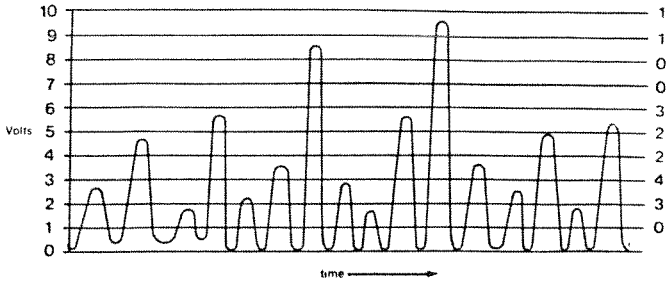
A better term for Pulse Height Analysis would be Pulse Height Distribution Analysis, because the input pulses are sorted by voltage amplitude to yield a histogram representing frequency of occurrence versus pulse height. A pictorial representation of this process can be seen in Figure 1-2.

Figure 1-2a depicts a series of voltage pulses as they might appear at the input to the Series 40. The vertical axis has been divided into ten (10) equally spaced intervals, each representing one volt of pulse height. At the right of the figure the number of pulses falling into each of the various intervals is tabulated. This same data is then shown in histogram form in Figure 1-2b, where the horizontal axis divisions correspond to the voltage divisions on the original signal. It is this type of pulse height distribution analysis that is performed by the Series 40 MCA during PHA mode data acquisition.

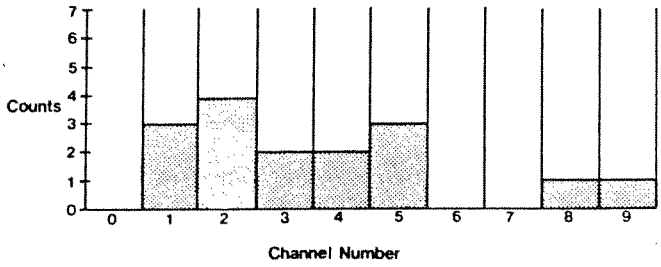
The primary application of PHA operation is in the quantification of the output signals from the class of radiation detectors whose output is a current or voltage pulse proportional in amplitude to the energy absorbed by the detector. Typical of such detectors are Scintillation detectors such as NaI(Tl), Semiconductor detectors such as Ge(Li), HPGe, or Si(Li) and Gas Proportional detectors.

A common characteristic of all these detectors is that each current or voltage pulse produced by the detector corresponds to the energy deposited by an individual photon or particle. Since the nuclear or atomic decay which generates the incident radiation is a randomly occurring process, the pulse train from the detector to the Series 40 is a time-random mixture of pulses of all possible amplitudes. The job of the Series 40, in PHA operation, is to sort this pulse train by amplitude and store the resultant spectrum. This can be seen graphically in Figure 1-3, where both the detector output and PHA histogram for a Cobalt-60 source are shown.

The 1024 channel histogram shown in Figure 1-3b is directly analogous to the ten channel histogram in Figure 1-2b but is of far greater resolution. That is, the input pulses have been sorted into 1024 discrete amplitude levels rather than just ten levels. Each point in the Figure 1-3b display represents the number of counts accumulated in one particular channel; it is still a pulse height distribution histogram.



a. Input Voltage Pulses



b. PHA Histogram

Figure 1-2
PHA Operation

From an analytical point of view, a PHA distribution histogram (spectrum) can provide both qualitative and quantitative results. Since channel number corresponds to input voltage, and input voltage corresponds to the energy of the radiation striking the detector, the energy of any peak in the spectrum can be easily determined; and from the energy (or energies) present one can determine the source.

The spectrum can also yield quantitative data. Since all measurements of radiation intensity are based upon the number of events per unit time, one need only divide the number of occurrences of a given energy by the total acquisition time to get a measure of the activity present. This is, of course, an oversimplification, since there are many other physics-related factors that must also be considered. But conceptually, the principle of "counts divided by time" is valid.

Because of this, when operating in PHA mode, the Series 40 stores acquisition time along with the spectral data. Channels 0 and 1 of the Series 40's memory are reserved for the time storage function. Channel 1 stores true (real) time.

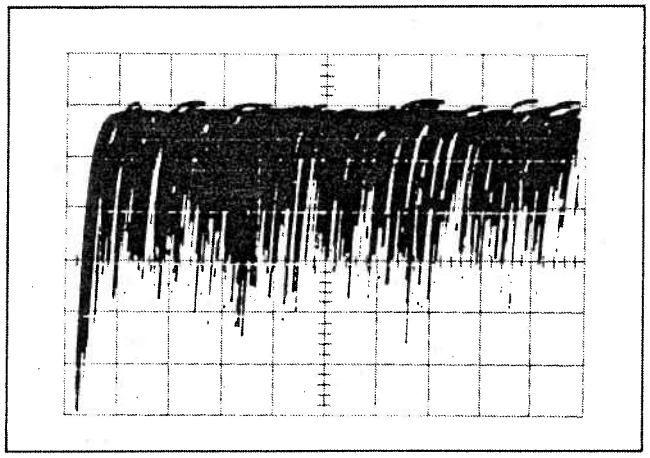
The time value stored in channel 0 is generated by a special circuit called a "live time clock", and the value accumulated is called the "live time". The need for this special time circuit can be seen by examining in closer detail the operation of the Series 40 PHA in relation to the input pulse train.

From a time standpoint, the input pulse train is totally random in nature. Therefore, since it does take the analog-to-digital converter (ADC) a finite amount of time to convert a pulse amplitude into a channel number, some

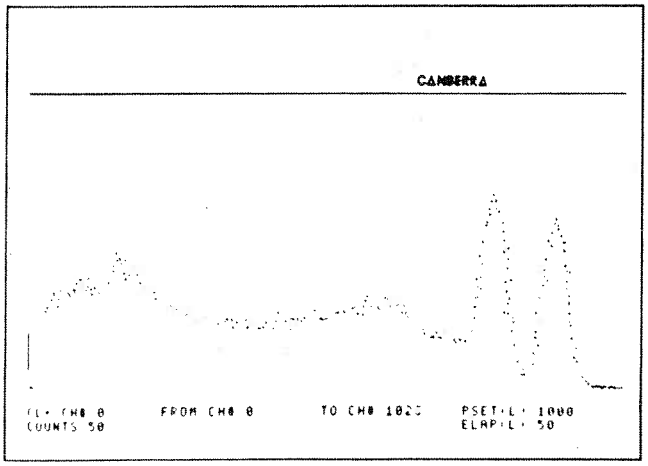
pulses will arrive at the ADC only to discover that it is busy processing the previous pulse. The ADC is effectively "dead" and this datum (pulse) is lost.

Because of this "dead-time" phenomenon, a time correction circuit is required to compensate for the fact that the number of input pulses per unit time can vary considerably from the number of events stored per unit time. This time correction circuit, called the "live time clock", extends the total elapsed counting time to compensate for the percentage of time that the ADC is "busy". This circuitry can be seen in operation via the % Dead Time bar-graph at the top of the Series 40's display.

For PHA operation, the primary goals are, therefore, the ability to measure the distribution of input pulse heights and to keep track of the system live counting time. The time function is automatically handled via the live time clock and requires no parametric input. However, the Series 40 does provide several methods for modifying the parameters of the pulse height distribution function.



a. Voltage Train Output from NaI Detector



b. Resultant Series 40 PHA Histogram

Figure 1-3
Pulse Train Conversion to a PHA Histogram

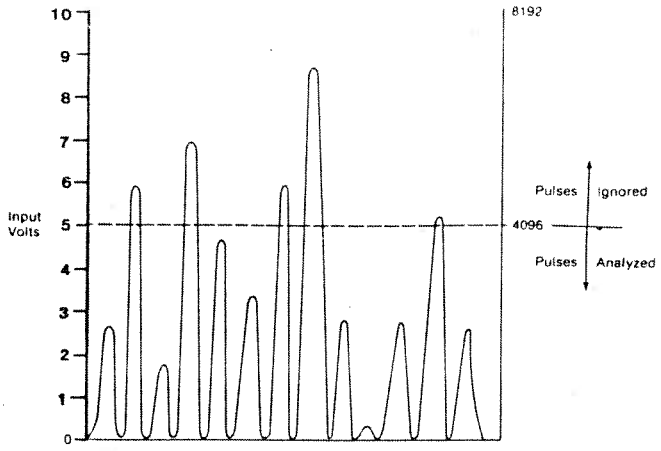


Figure 1-4
Effect of 8192 Conversion Gain and 4096 Channel Memory

1.2.1.1 ADC Gain

One of the factors affecting the generation of a pulse height distribution histogram is the system resolution; that is, the number of discrete voltage levels - or channels - into which the input pulses will be sorted. In ADC terminology, this is called the ADC Conversion Gain. For example, our initial histogram (in Figure 1) used ten separate one-volt levels for sorting; it had an ADC Gain of 10.

For most PHA operations, the intent is to analyze the input voltage over its entire 0 to 10 volt range. To do this with maximum resolution, the ADC Gain is set equal to the Memory Size. This corresponds to an ADC Gain of 4096 channels on the Series 40 (Model 4202).

Alternatively, an ADC Gain of 2048 channels would allow two separate spectra to be stored in either half of the 4096 channel memory.

1.2.1.2 Digital Offset

For situations requiring greater resolution, the Series 40 ADC provides an ADC Gain of up to 8192 channels. However, since the Model 4202 memory provides only 4096 channels of storage, only a portion of the input voltage range can be examined at one time using the 8192 channel ADC resolution.

If one were interested only in the first five volts of the zero to ten volt input range, the experiment setup would be quite straightforward, as shown in Figure 1-4. Pulses below the five volt (channel 4096) level are analyzed and stored; those above are ignored.

But what if the objective is to analyze those pulses in the five to ten volt range: how can this be accomplished? It is in this situation where the value of ADC Offset can be seen.

Up to this point, it has been assumed that ADC channel numbers and memory channel numbers are the same. In reality they are independent, and it is the ADC Offset control which establishes their relationship.

When the ADC and memory channel numbers are the same, the ADC Offset is said to be zero. This relationship can be shifted linearly via the ADC Offset control. For example, to analyze the upper five to ten volt range of the input using a 8192 channel ADC Gain and a 4096 channel memory, what is needed is to "shift" the zero channel of the memory to correspond to channel 4096 of the ADC. In other words, an ADC Offset of 4096 channels is required. The Series 40 includes 32 different ADC Offset settings to allow the selection of the optimum value for any given situation.

1.2.2 Multichannel Scaling

MCS analysis yields a histogram representing number of events (radiation intensity) versus time. Just as in PHA, the input signal is a train of pulses, each representing a single event. However, MCS analysis does not concern itself with the amplitude of these pulses; the data stored is simply the number of individual pulses which were received in a given period of time.

As pulses are detected at the input of the Series 40, MCS mode operation counts them one-by-one into the current memory channel for a predetermined period of time. At the end of this time period, which is called the dwell time, the MCS time base advances to the next memory channel address. Pulses are now counted into this channel for the dwell time period. Each memory channel is thus sequentially selected as a function of time.

This operation can be seen in a simplified form in Figure 1-5. The input pulse train in 1-5a would generate the histogram shown in 1-5b. Note that an MCS analysis produces an integral histogram; each channel represents the summation of all counts within the given time period and not the instantaneous count rate.

MCS analysis finds use in several applications involving the study of the distribution of events as a function of time. One such application is the study of nuclear decay; the resultant MCS histogram represents the exponential decay curve.

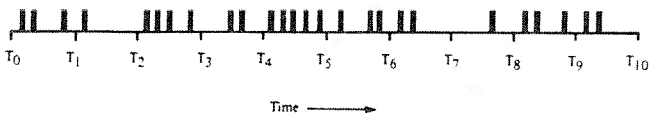
Many other applications - such as Mossbauer spectrometry - involve the synchronization of the MCS scan to an external device. In this case, the time axis really relates to an external device position or condition, such as source velocity in the case of Mossbauer work.

For all applications an appropriate dwell time must be selected prior to the analysis. Several factors can influence this choice.

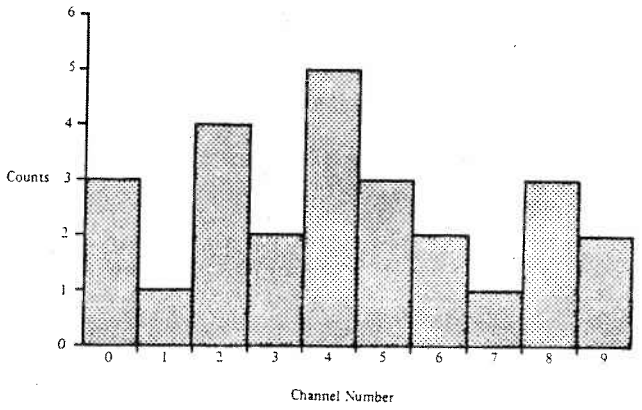
1. Desired time for the entire scan.
2. Number of channels to be used for data storage.
3. Desired counting statistics (number of counts per channel).
4. Operating rate of an external device.

In many cases, several of these criteria may be incompatible. For example, the sweep rate of a Mossbauer spectrometer may be too rapid to allow collection of adequate statistics in a single data acquisition scan. For these situations the Series 40 provides an MCSR operating mode, which allows recurring, or multiple, MCS acquisition sweeps.

Depending upon the external device being used, it may be necessary to synchronize these recurring sweeps to the mechanical motion. The Model 4232 External Control Wiring option provides this capability.



a. Input Pulse Train



b. MCS Histogram

Figure 1-5
Multichannel Scaling

Section 2.
Basic Series 40 Operation

2.1 Power On

This section describes the operation of the Series 40 Multichannel Analyzer and the basic dialogue rules

Power is applied to the Series 40 with the ac power switch on the analyzer's rear panel. Before applying power, check the voltage selection card inside the fuse compartment on the rear panel. This is easily done by moving the plastic fuse shield to the left and looking directly under the fuse; the operating voltage will be visible. Should it be necessary to change the operating voltage, refer to Appendix A.1 for instructions.

The analyzer will be set for either 50 Hz or 60 Hz operation. If it should be necessary to change line frequency, refer to Appendix A.2 for instructions.

The intensity of the display is controlled by the INTENSITY potentiometer located on the left side of the Keyboard. A few seconds after power on, the display will appear and will look as shown in Figure 2-1. This System Initialization state shows the internal clock time starting at 00:00 and the date on which the installed firmware was released to production.

Note that the LED indicators for PHA and ADD on the Control Panel are illuminated. The analyzer's default state assumes that the most common operating mode will be used; changing these modes is done by pressing a pushbutton for another mode. See Section 4 for examples.

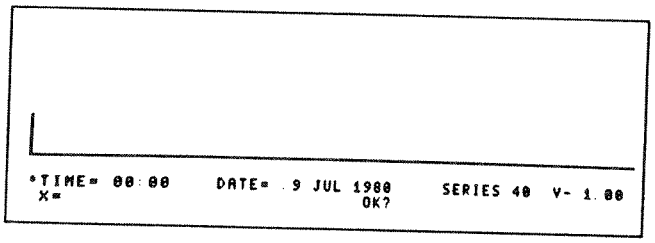


Figure 2-1
Initial Display

The usual first step after power is applied is the setting of the clock and the calendar to current values. If new values are not entered, the clock and calendar will keep time from 00:00 of the firmware release date.

The procedure for entering new values is as follows:

1. Using the numeric keypad on the right side of the Keyboard, enter the correct time in the form Hours.Minutes on a 24 hour basis. Note that the value if first entered in the X Register.

2. If an error is made in the entry, the red CLEAR key on the keypad can be used to erase the value of X. A new value may then be entered in the X Register.

3. Press STORE on the keypad to transfer the entry from the X Register to the TIME variable.

4. Press NO to move the * to DATE and enter the new value for the date in the form DD.MM.YY and press STORE. Note: The year must be entered using the year's last two digits only. That is, 1981 is entered as 81.

5. Press YES (in answer to the question OK?) to have the new values accepted and the system revert to a normal display (Figure 2-2).

2.2 System Initialization

Associated with the Expand and Integrate functions is the Power Reset command. It is activated by simultaneously pressing these two pushbuttons. Issuing a Power Reset command aborts any operation in progress but does not alter any time or data information nor does it alter any operator-set parameters. Power Reset does not normally need to be used to abort an operation because all operations can be terminated simply by turning the function off.

Performing a Power Reset causes the display to revert to the initial power-on display seen in Figure 2-1 and thus can be used to check the status of the system time and date clock and the Firmware version. Answering YES to the question OK? will return the system to the normal display.

Note that the Power Reset has returned the system to the initial PHA/ADD state from any other data acquisition mode previously selected.

2.3 Basic Dialogue Procedures

The brief process of entering the current time of year, described in the previous section, illustrates many of the basic dialogue "rules" common to all Series 40 operations. As the remainder of the manual is read, many additional examples will be seen. The following is a summary of those rules which are, in general, applicable to any dialogue sequence.

1. If a dialogue sequence is capable of accepting a numeric parameter, the X Register (X=) will be displayed on the lower left portion of the CRT.

2. During the entry of a numeric parameter, it is displayed as it is typed in the X Register. Errors may be corrected by touching CLEAR and re-entering the value.

3. Touching STORE causes the entry in X to be evaluated and transferred to the parameter field being modified.

4. A numeric entry, up to 16 displayed characters, can be entered as an arithmetic operation. For instance, 5120 can be entered as X = 4096 + 1024. This entry will be evaluated and stored as 5120 when the STORE key is pressed.

5. The parameter field currently selected for modification is the one adjacent to the blinking *. To select a different parameter for modification, the

blinking * must be moved to the desired parameter field.

6. When several choices are listd on a line, touching NO moves the blinking * to the next parameter in sequence on the line.

7. When the question NEXT? is displayed, touching YES will mean "what is displayed is acceptable; go on to the next step." When the question OK? appears, YES will mean "I agree; end the dialogue."

8. If a dialogue procedure is aborted (by turning off the function rather than answering all questions), all original values are maintained as if the function was never started.

9. An illegal entry will generate an error message. To proceed, touch CLEAR on the numeric keypad and re-enter the correct value.

10. Under some conditions, a numeric display may show either a series of asterisks (**) or, in later Firmware versions, a series of "greater than" signs (>>). This indicates that the number is too large for the display area; the number will be correctly stored in memory.

The Series 40 also offers an additional operating characteristic that most users will find very beneficial after some "hands on" experience is gained: Console Function Type-ahead. That is, as buttons are pushed, the code for each is stored in list (on a First In, First Out basis) and then retrieved in sequence for execution. This allows an operator who is familiar with a procedure to quickly touch all needed buttons, in the correct sequence, without waiting for the displayed dislogue to "catch up".

2.4 LED INDICATORS

Most of the pushbuttons have a built-in light-emitting diode (LED) indicator to show the status of the associated function. The few pushbuttons lacking an indicator are "momentary" functions; that is, the function does not remain enabled after the pushbutton is released.

When any pushbutton with an indicator is pressed, the function is enabled, and the LED is illuminated to show the status of the function. Pressing the pushbutton a second time will disable the function, turn off the indicator, and abort any process that was initiated when the function was enabled.

Note that any prerequisites must be fulfilled before some of the functions can be enabled. For example, OVLAP cannot be enabled usless the MEMORY switch is in a position other than 1/1.

2.5 SIGNAL CONNECTORS

Figure 2-2 illustrates the three BNC type signal connectors. Two of these, labled ADC IN and AMP IN, are analog signal inputs. The other connector, labeled GATE IN, accepts logic signals to condition the ADC to either accept or reject analog signals for conversion. See Section 2.6, following, for information concerning use of the GATE input.

The AMPlifier INput can route signals from an external preamplifier to the internal amplifier or from a detector to the internal preamplifier. The ADC INput accepts 0 to 10V signals from an external amplifier which can then be processed by the ADC.

The adjacent ADC IN switch must be in the correct position for the input connector used. The AMPlifier position allows signals from the internal amplifier to be routed to the ADC; the EXTernal position connects the ADC INput connector directly to the ADC, bypassing the internal amplifier.

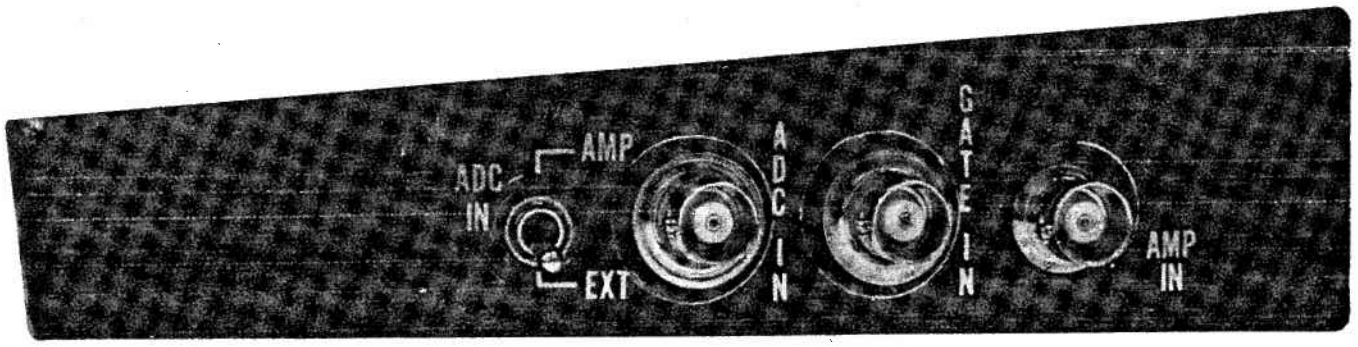


Figure 2-2
Signal Connectors

Care should be taken to keep the signal cables away from the CRT because it is possible for the CRT to induce noise on these input lines.

The rear panel has a number of other connectors. Their uses will be covered in Sections 7 and 8.

2.6 GATE

The GATE function allows the operator to enable or disable the ADC for acceptance and conversion of linear signals at its input. Depending on the criteria for the experiment in progress, the operator may use the GATE input in the factory-set coincidence mode or may change the function to the anticoincidence mode by moving a jumper on the ADC board (see Appendix A.3).

The GATE input signal must be coincident in time with the linear signal in order to be considered by the ADC regardless of the mode chosen.

In the Coincidence mode:

1. A low logic level (0 to 0.8 volts) at the GATE connector will disable the ADC. It will neither accept nor process any linear signals while the GATE is low.

2. A high logic level (2.5 to 5.5 volts) at the GATE connector will enable the ADC. It will accept and convert all linear signals received while the GATE input is high.

3. If the GATE input is left open (unconnected), the ADC will act as if the GATE Input is high and will accept and convert all linear signals received.

In the Anticoincidence mode, the logic is reversed. That is, a low logic level will enable the ADC and a high level (or an open input) will disable the ADC.

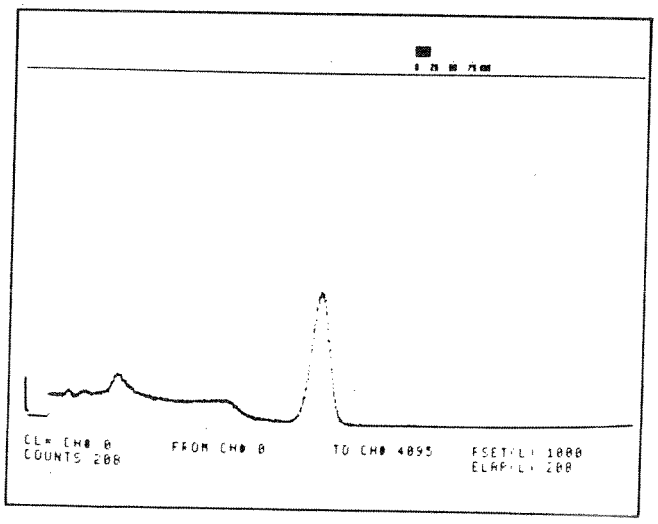


Figure 2-3
Typical PHA Spectrum (NaI detector)
showing Dead Time bar graph

2.7 INPUT

The Series
an external
from the AM

The Analyz
detector, as
moving a ju
Moving the
internal pre
amplifier.

2.8 POSIT

In the Voltag
factory-set f
A.3 for ins
negative-go

2.9 SAMPL

In the Samp
voltages (dc
sampled by
distribution
signal and n
ULD control

The GATE i
must be coir

To use the ar
jumper on th
position. See
PHA mode,
position.

2.10 DEAD

Any signal th
the ADC is p
ADC. This is
previous sig
finished with
Dead Time.

The Dead Ti
moving bar
COLLECT m

Note that any
the factory se
even though

Section 3.
Using PHA and MCS

This section will outline two possible experimental setups using the Series 40 and either a charge sensitive input (from a scintillation detector, such as Canberra's model 802 series) or a voltage sensitive input (from any other type of detector). See Appendix A.3 for instructions on changing from one type of input to the other. If a scintillation detector is connected to an external preamplifier the preamp's output can be connected to the Series 40 as a voltage sensitive input.

3.1 SETUPS

For a charge sensitive input, the following equipment, or equivalent, will be required:

- Series 40 MCA
- Model 3100-01 or Model 4261 High Voltage Power Supply (HVPS)
- Model 802 series Scintillation Detector
- Model 2007 Photomultiplier Tube Base
- Cables for interconnection as shown in Figure 3-1.

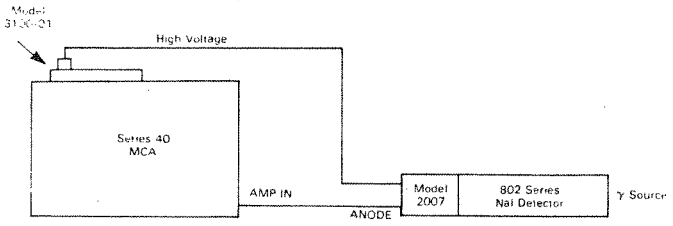


Figure 3-1
Charge Sensitive System Setup

For a voltage sensitive input, the following equipment, or equivalent, will be required:

- Series 40 MCA
- Model 4261 High Voltage Power Supply (HVPS)
- Model 4225 Spectroscopy Amplifier; NaI detectors can use the internal amplifier.
- A Ge(Li) detector with a Model 2001 Preamplifier or a Model 802 Detector with a Model 2007P Preamplifier.
- Cables for interconnection as shown in Figure 3-2.

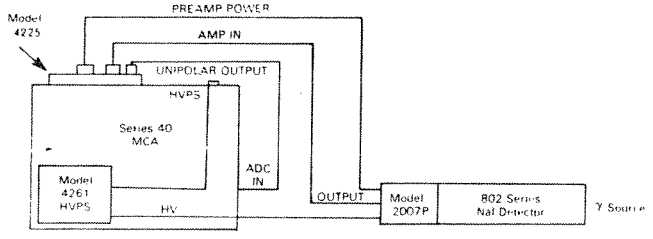


Figure 3-2a
Voltage Sensitive System Setup (NaI)

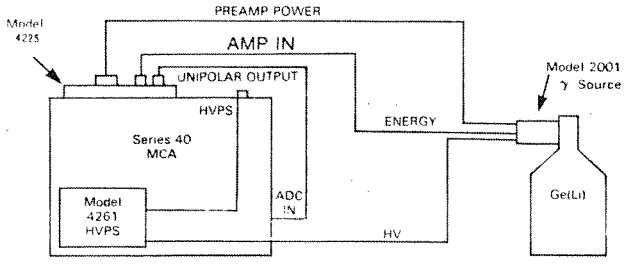


Figure 3-2b
Voltage Sensitive System Setup [Ge (Li)]

3.2 DATA ACQUISITION

Initial Control Panel Settings:

ADC IN SWITCH	AMP (EXT IN for Figure 3-2a)
VERTICAL RANGE	1K or LOG
MEMORY	1/1
ADC GAIN	1024 for Model 4201 4096 (for Model 4202) 8192 (for Model 4203)
ADC OFFSET	None: all switches down
SCA LLD	0.20
SCA ULD	Fully clockwise (10)
MODE	PHA and ADD (default state).

1. Turn on the Series 40 with the ac power switch, set time and date if desired and press YES.
2. Turn on the HVPS with its separate switch.
3. Set the HVPS to the correct operating voltage for the detector being used.
4. Place a radioactive source near the face of the detector.
5. Press COLLECT to start data acquisition. Note that the LED indicator is illuminated in the COLLECT pushbutton, showing that acquisition is in progress. Note the Dead Time meter displayed at the top of the screen.
6. Adjust the AMPLIFIER GAIN so that the spectrum (data being displayed) is positioned conveniently on the display.
7. Pressing CLEAR DATA repeatedly while adjusting the AMP GAIN will aid in positioning the spectrum.
8. Allow the data to accumulate for a few minutes.
9. Press COLLECT again to stop acquisition. Note that the LED indicator is no longer illuminated.

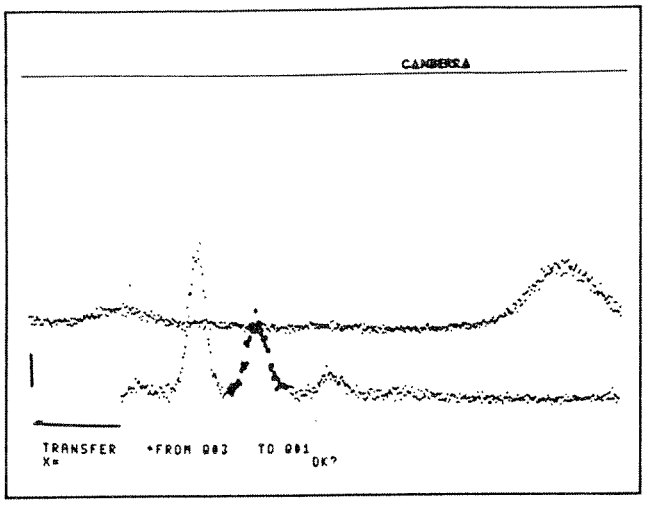


Figure 3-3
Transfer Dialogue and Display

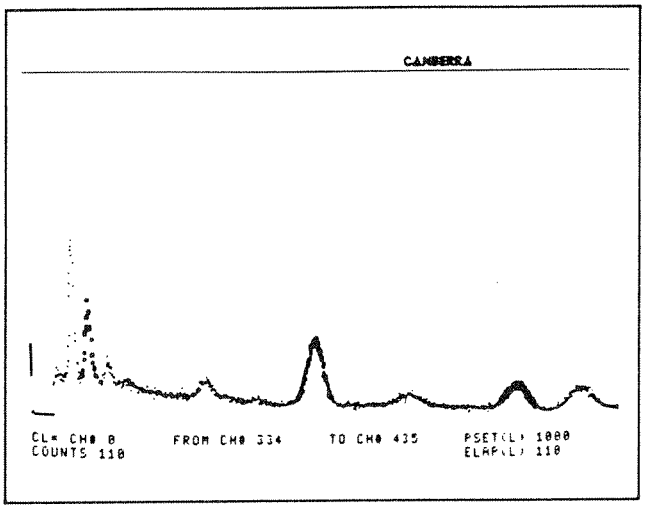


Figure 3-4
NaI Spectrum with 3 ROI's Entered

3.3 DATA MANIPULATION

To see the effects of some of the Keyboard functions:

1. Change the MEMORY switch to 1/4.
2. Press XFER. Note that the dialogue asks if the operator wants to transfer Q # 3 to Q # 1 (memory quarter number three to memory quarter number one). The contents of Q # 3 are displayed above the contents of Q # 1.
3. Press YES to enable the transfer. Note that the upper data trace is no longer displayed and the data has been copied into the memory section being viewed (Q # 1).
4. Press OVLAP. Note that the MCA displays the two quarters with the upper data offset by 20% above the lower data, as in step 2. The dialogue asks "Q # 3 over Q # 1 OK?". Pressing YES will terminate the overlap dialogue, but the overlapped data will still be displayed.
5. Press OVLAP again to disable the function. Note that the display returns to normal; that is, the overlapped data is no longer displayed.
6. At the bottom of the Keyboard is a double headed arrow. The two buttons within the arrow heads are the cursor scan controls, which move the cursor to the right or to the left through the spectrum. Press the Scan right button and watch the cursor move slowly to the right and then gradually move faster. When the cursor is at the beginning of a peak in the spectrum, release the Scan button to stop cursor motion.
7. Press ENT ROI and Scan the cursor to the right again. Note that the data points in the peak are intensified as the cursor moves through them.
8. Release the Scan button and press ENT ROI once more to disable the function. A Region of Interest has now been entered around the peak. Repeat steps 7 and 8 for several more peaks.
9. Press INDEX and watch the cursor jump from the beginning of one ROI to the beginning of each succeeding ROI in turn. Note that the cursor will index from the last ROI in the spectrum to the first ROI. This is what is meant by "around the corner" indexing.
10. Press EXPAND to see the display change to include only 128 channels, with the cursor at the 25% point of the Expanded display.

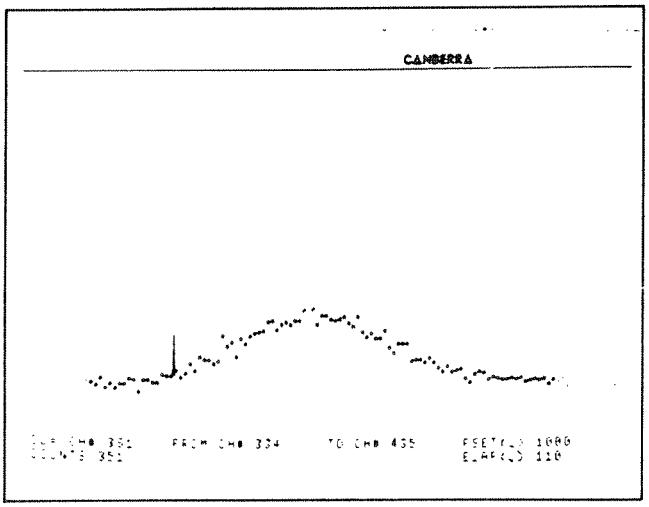


Figure 3-5
An Expanded ROI

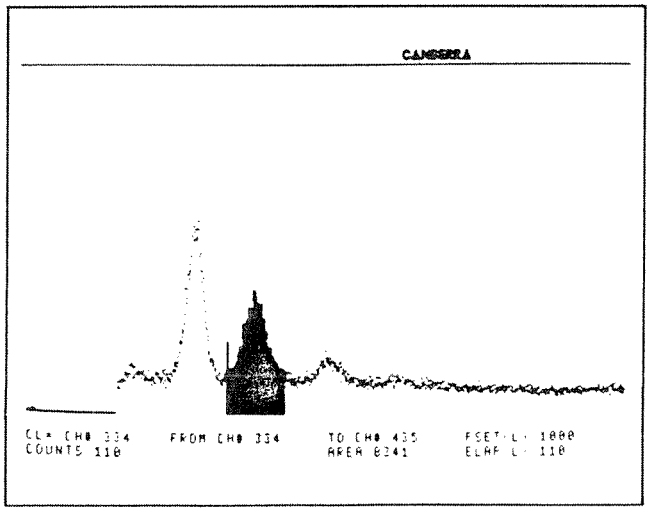


Figure 3-6
An ROI with AREA Enabled

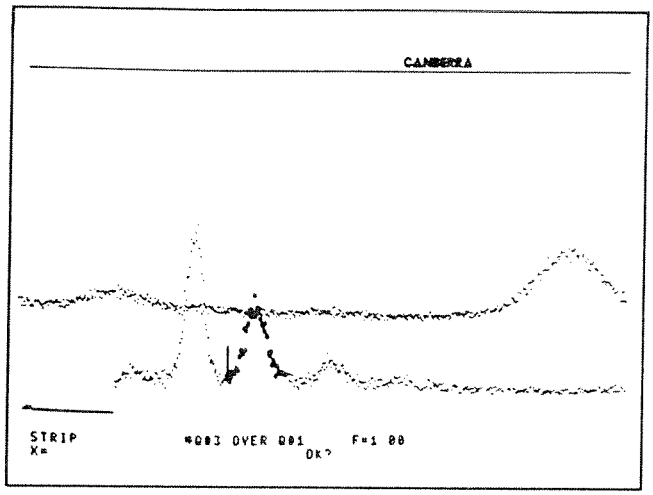


Figure 3-7
Strip Dialogue and Display

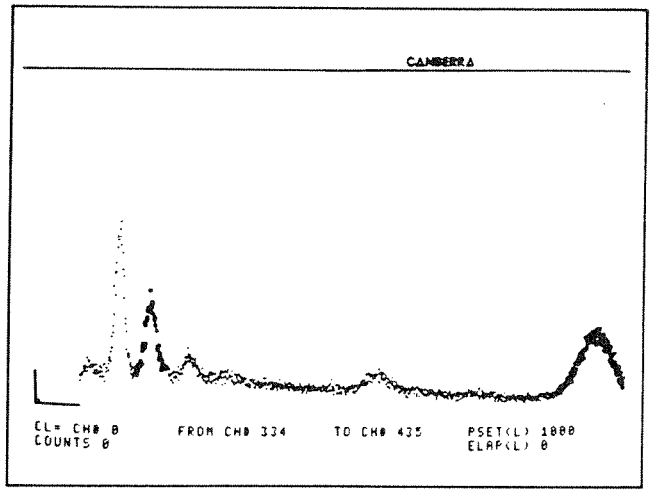


Figure 3-8
Clear Time Performed, Channel 0 has Zero Counts

11. Press ROLL and then scan the cursor to the right. Note that the cursor stays centered in the display and the data appears to move to the left as the 128-channel window is scanned to the right through the spectrum.
12. Press EXPAND again to disable the function. Note that the ROLL function is disabled simultaneously.
13. Press INDEX to put the cursor in an ROI
    Press AREA and note that the ROI now has vertical histogram bars entered from the baseline to the data point in each channel in the ROI. The value of the area is shown at the bottom of the screen. Press AREA again to disable the function.
    Press INTEG to compute the integral value of the ROI. Make a note of the value as displayed at the bottom of the screen. Disable INTEG.
    Press STRIP. Observe the flashing * in the dialogue. Press NO to advance the * to F 1.00.
17. Change the value of the factor (F) by entering a decimal point, the numeral 5 and pressing STORE. F should equal 0.5.
18. Press YES to allow the Strip to proceed. The display will flash BUSY! at the bottom of the screen while the Strip is active to indicate that the analyzer is unable to perform any other functions until the function in progress is complete.
19. Observe that the display shows both quarters as in OVLAP. Watch the stripping progress through the lower spectrum. The MCA is multiplying the data in Q # 3 by the factor (0.5) and subtracting the result from the data in Q # 1. The result is the reduction of the data in Q # 1 by one-half. This can be verified by enabling INTEG once again and comparing the displayed integral to the value noted in step 15; it should be about one-half of that noted value.
20. The data displayed in Q # 1 can be read out to a peripheral device by using the READ OUT function. See Section 6, Input/Output, for instructions.
21. Press HOME. Note that the cursor has returned to channel 0, the first channel of the displayed segment.
22. Press CLEAR TIME. Look at the counts displayed for channel 0 (CL counts) and the ELAP (L) on the lower part of the display. Both should now read 0 (time has been cleared from memory). No data channels are affected by this function.
23. Press CLEAR DATA and note that all data has been cleared from memory. This function clears only the displayed section of memory, other sections are not affected by the operation. If CLEAR TIME had not been performed in the last step, enabling CLEAR DATA would have reset the two time channels, as well as all of the displayed data channels, to zero.

3.4 MCS MODE

To see effect of MCS operation, use the same setup and control settings as for the preceding PHA experiment.

1. If there are data in the memory, press CLEAR DATA.
2. With the sample near the memory, press COLLECT.
3. Increase the LLD control setting until no pulse storage takes place below the energy of interest, such as one or more of the peaks. Repeatedly pressing CLEAR DATA while increasing the LLD control will aid in finding the desired setting.
4. Lock the LLD control, press COLLECT to stop acquisition and press CLEAR DATA to clear the memory.
5. The ULD control can be decreased in the same manner if data acquisition is not wanted above a specific energy level.
6. Press MCSR (for multiple sweeps through memory).
7. Press COLLECT and observe the type of data displayed as a result of this different type of acquisition.
8. Press COLLECT to stop the MCS sweeps.

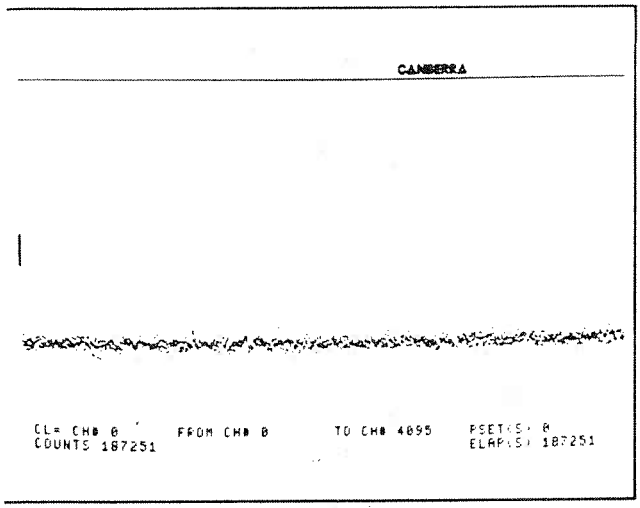


Figure 3-9
Typical MCSR Spectrum after 187 251 Sweeps

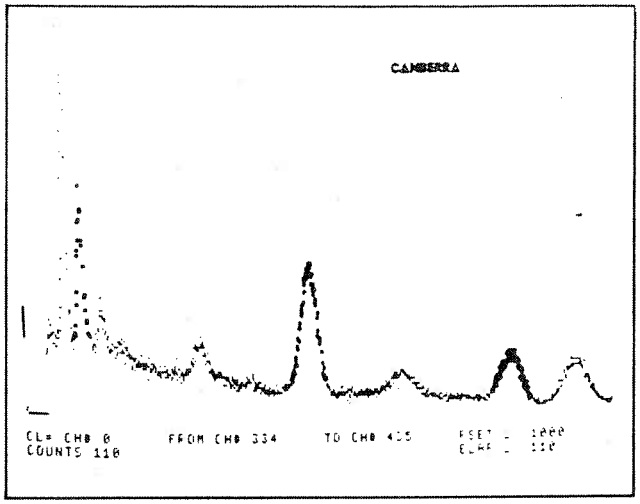


Figure 3-10
X2 Enabled. Note that the Horizontal Line of the top of the Display is absent.

Section 4.
Front Panel Functions

This section covers the controls found on the vertical Front Panel. These controls are concerned with the tasks of data acquisition and data input/output. Figure 4-1 provides a ready reference to the Control Panel layout.

The controls on the Keyboard (the horizontal panel) are used primarily in data manipulation and analysis. The description of their functions is covered in Section 5, following.

Starting with the functions in the upper left corner of the Front Panel, the controls are discussed as related groups from left to right and from top to bottom.

4.1 VERTICAL RANGE AND X2 GAIN

This eight position rotary switch selects the desired full-scale count value for the display, from 256 to 1048K (1 048 575) counts per channel, plus LOGarithmic display. Note that the highest setting is 2^{20}-1 counts.

The switch is normally set so that the highest peak in the spectrum is no higher than the top of the display. If a channel accumulates more counts than can be displayed, the channel will "overflow." This is seen as a peak which appears to have its top cut off and is increasing in height again from the baseline. If a channel overflows the VERTICAL RANGE setting, the operator must increase the VERTICAL RANGE setting.

The X2 GAIN function multiplies the vertical display by 2 and provides an intermediate step in the full-scale ranges selected by the VERTICAL RANGE switch. 256 X2, for instance, gives a vertical viewing range of 128 counts per channel.

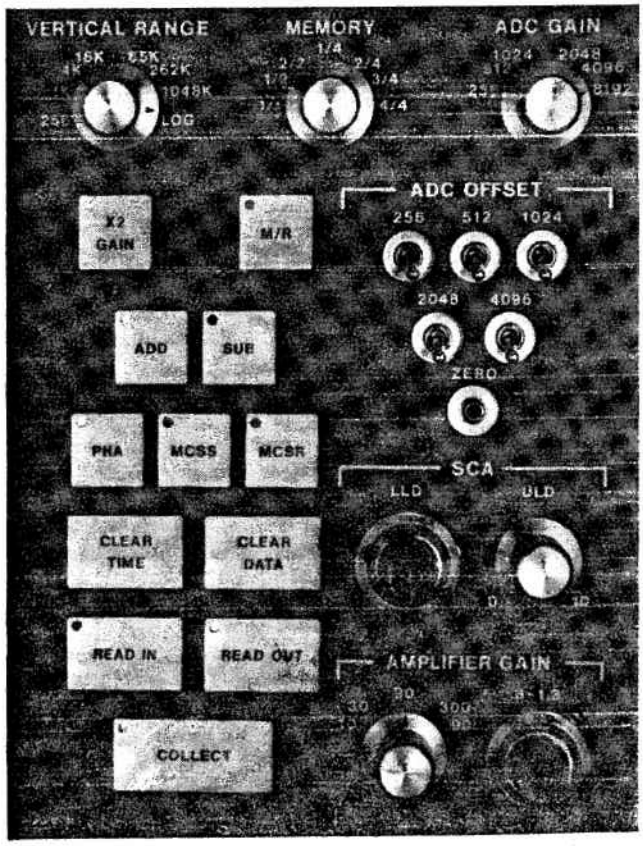


Figure 4-1
Front Panel

4.2 MIXER/ROUTER

If the Model 4231 Mixer/Router Wiring or Model 4223 Multi-ADC Interface is installed in the analyzer, pressing the M/R button will allow the operator to choose how many inputs the analyzer is to accept. The dialogue will read:

NO. INPUTS *2 4 8 16
OK?

Note: an Analyzer with a 1K memory will not offer the choice of 8 or 16 inputs.

Choosing the number of inputs with the * will cause the Firmware to divide the full memory into the selected number of equal parts for separate data storage for each input.

To use the Analyzer with one input, the M/R button should not be used. If a Model 8220A Mixer/Router is being used, it should be disconnected from the system when a single input is desired.

Refer to the Model 8220A Mixer/Router's Operator's Manual or to the Model 4223 Multi-ADC operating instructions for further information.

4.3 MEMORY

The MEMORY switch selects the section of memory to be:

- addressed by the ADC for data storage
- displayed by the CRT
- read out of or read into

The operator may select full memory, either half or any of the quarters.

- 1/1 refers to the full memory
- 1/2 refers to the first half of the memory
- 2/2 refers to the second half of the memory
- 1/4 refers to the first quarter of the memory
- 2/4 refers to the second quarter
- 3/4 refers to the third quarter
- 4/4 refers to the fourth quarter

Regardless of the memory segment chosen, the first two channels of the segment are used to register PHA Live and True time or MCS sweep count and Dwell Time code.

4.4 ADC GAIN

This six-position rotary switch is used to establish the full scale resolution of the ADC, as discussed in the Introduction (Section 1.2.1.1). The ADC Gain is commonly set to equal the number of channels memory; that is, a 4K memory (4096 channels) would commonly use an ADC GAIN of 4096.

For finer resolution over a narrower energy range, the ADC GAIN switch, in conjunction with the ADC OFFSET, can be used to display the energy range of interest.

4.5 ADC OFFSET

The ADC OFFSET establishes the relationship between memory channel zero and the ADC channel assignments. The effect of the Offset is to shift the spectrum by a selected number of channels.

For instance, if an ADC GAIN of 4096 is selected but only 1024 channels of memory are being displayed, then the upper 75% of the spectrum will not be stored in the memory. If the upper 25% of the spectrum is to be stored in the memory, the ADC OFFSET will have to be changed from zero to some number that will shift the spectrum by the desired number of channels.

In this example, an Offset of 3072 (1024 + 2048), which is the 4096 Gain less the 1024 memory size, will accomplish the shift by moving the zero channel of memory to ADC channel 3072. Converter pulses whose value is < 3074, will be discarded and pulses which convert to 3074 will be stored in the first data channel of the memory (channel 2). Note that the offset switches are additive.

With ADC Gains of 512 or 256, the Offset indicated by the switches is divided by 2 or 4, respectively.

4.6 ZERO

The Analyzer is shipped with the ZERO control set for the memory size installed.

The ZERO control is a screwdriver-adjustable potentiometer which shifts the ADC zero relative to a zero energy (0 volts) input. This is done by shifting the spectrum by up to 5% of the ADC GAIN being used. It can be used like the ADC OFFSET to provide a fine control for positioning peaks.

The ZERO should be recalibrated each time the ADC GAIN is changed but is not critical. The result of not readjusting the ZERO will be a slight shift in the spectrum's peaks and slight change in linearity.

When performing experiments which require better linearity, channel zero of the analyzer is usually made to correspond to zero energy input. Appendix C lists three methods for accurately setting the ZERO control.

4.7 ADD AND SUBTRACT

These two buttons enable either additive or subtractive data acquisition. If ADD is enabled, all new data acquired is added to existing data in the memory.

If SUBtract is enabled, all new data is subtracted from existing data in the memory. This mode is useful for subtracting a background or a standard reference spectrum from a previously acquired spectrum. Channels 0 and 1 are always additive.

The Series 40 default (power on) state automatically enables the ADD mode of data acquisition, as does System Initialization (see Section 2.2).

4.8 PHA
Selects the Pulse Height Analysis (PHA) mode of data acquisition. Used in combination with either the ADD or the SUBtract mode (Section 4.7 above). See Section 1.2.1 for a description of the PHA function.

The Series 40 default (power on) state automatically enables the PHA mode, as does the Power Reset command.

4.9 MCSS
Selects the Multichannel Scaling Single sweep (MCSS) mode of data acquisition. See Section 1.2.2 for a description of this mode. Used in combination with either the ADD or the SUBtract mode (Section 4.7 above).

If MCSS or MCSR acquisition is in progress, the firmware allows the operator to "STOP" or "ABORT" when terminating COLLECT. STOP = terminate at the end of the current sweep; ABORT = terminate immediately. ABORT is given as a choice only when the selected dwell time is equal to or greater than 2 msec.

4.10 MCSR
Selects the Multichannel Scaling Recurring sweep (MCSR) mode of data acquisition. See Section 1.2.2 for a description of this mode, which differs from the MCSS mode only in that the analyzer will continue sweeping through the memory for a preset number of sweeps (see Section 5.2.2, MCS Preset) rather than a single sweep as in MCSS. Used in combination with either the ADD or the SUBtract mode (Section 4.7 above).

If MCSS or MCSR acquisition is in progress, the firmware allows the operator to "STOP" or "ABORT" when terminating COLLECT. STOP = terminate at the end of the current sweep; ABORT = terminate immediately. ABORT is given as a choice only when the selected dwell time is equal to or greater than 2 msec.

4.11 LLD (Lower Level Discriminator)
This ten-turn, locking potentiometer is used to establish the lower energy limit for input signals that are to be converted by the ADC. Input signals that are below the LLD setting in amplitude are not converted. If signals below the LLD setting are above the factory set threshold, those signals will add an increment of deadtime equal to the signal's width.

For PHA operation, the LLD is usually set to a point just above the low energy noise that is normally present in the input signal. For MCS operation, the LLD is usually set just below the particular energy of interest.

4.12 ULD [Upper Level Discriminator]
A single-turn potentiometer which controls the upper energy limit for pulses to be processed by the ADC. Input signals that are above the ULD setting in amplitude are not converted.

For MCS operation, the ULD is usually set just above the particular energy of interest.

4.13 AMPLIFIER GAIN
The coarse and fine gain controls are provided to adjust the gain of the internal amplifier to the desired spectral energy range. Together they provide a gain range of 3 to 1170.

The coarse gain control is a five position rotary switch; the fine gain control is a ten-turn precision potentiometer that multiplies the setting of the coarse gain control by a variable factor which can be set as low as 0.3 or as high as 1.3.

The fine gain control is factory set to read 0.3 at its minimum setting so that its dial reads the variable factor directly, allowing the operator to set the amplifier's total gain with precision.

4.14 CLEAR TIME AND CLEAR DATA
These two pushbuttons are used independantly to either clear the first two channels in the memory segment chosen by the MEMORY switch (CLEAR TIME) or all channels in the chosen memory segment, including the time channels (CLEAR DATA).

CLEAR DATA is usually used to reset the entire memory to zero before starting a new experiment or a new run of the current experiment.

CLEAR TIME can be used to reset the two time channels to zero without erasing the existing data. The operator may wish to add or subtract new data using the same preset conditions as for the first data collection run.

4.15 READ IN AND READ OUT
These pushbuttons control the input/output flow of data from or to a peripheral data storage device, such as a Teletype, a Cassette Tape or a Plotter. Their use is covered in detail in section 6.

4.16 COLLECT
The COLLECT pushbutton controls data acquisition in the mode already chosen by the operator. (The PHA ADDitive mode, for instance.)

If MCSS or MCSR acquisition is in progress, the firmware allows the operator to "STOP" or "ABORT" when terminating COLLECT. STOP = terminate at the end of the current sweep; ABORT = terminate immediately. ABORT is given as a choice only when the selected dwell time is equal to or greater than 2 msec.

When Collect is enabled or disabled, the analyzer reads the position of the Memory switch to control data acquisition in that memory section. The Memory switch can then be changed at will in order to examine, manipulate or Read In/Read Out data in another section of memory.

Section 5.
Keyboard Functions

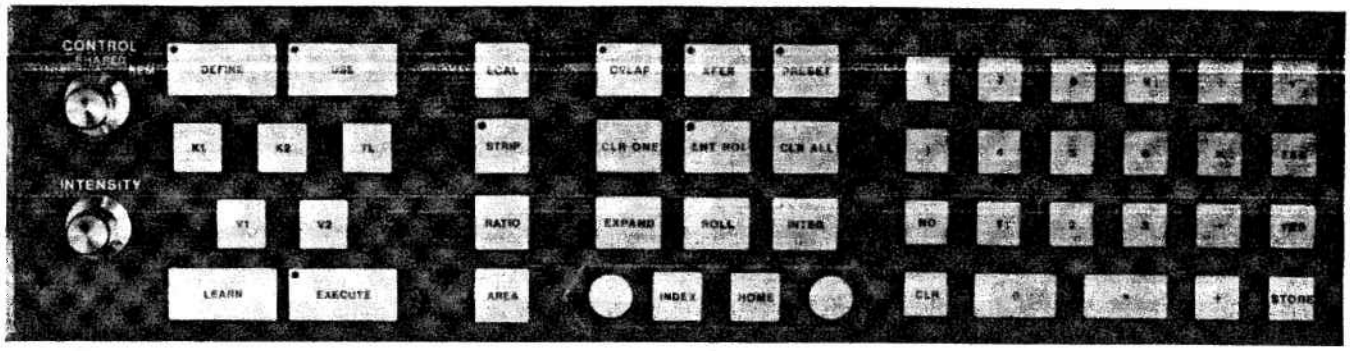


Figure 5-1
Keyboard Layout

The pushbutton functions on the Keyboard are concerned primarily with data manipulation. The pushbuttons on the left side of the Keyboard control the Model 4241 Define/Use option and the Model 4242 Learn/Execute option; the use of these options is covered in section 7.

Figure 5-1 provides a reference to the Keyboard layout.

5.1 KEYPAD

The right-hand one third of the keyboard is the keypad. It is used to enter numbers in the X Register and functions in the Define/Use option by means of the numerals zero through nine and the STORE and CLR (clear) keys. The STORE key transfers the contents of the X Register into memory and the CLR key erases incorrect entries from the X Register. The CLR key also aborts an ILLEGAL ENTRY and clears that message from the display.

Additional to these keys, the keypad has left and right parentheses "(" and ")", the four arithmetic operators, an exponential notation key "EEX" and a radical key "√".

5.2 CONTROL

The three position CONTROL switch is provided for the Model 4272 GPIB and the Model 4271 and 4273 Computer Interfaces only. If none of these is installed, the switch will have no effect.
If the Model 4271, 4272 or 4273 option is installed, the CONTROL switch will function as follows:

1. LOCAL—Allows only Keyboard control of the Series 40.
2. REMote—Allows only remote (Computer) control of the Series 40.
3. SHARED—Allows either Keyboard control or Computer control of the Series 40. Note that the analyzer cannot differentiate between Keyboard commands and Computer commands; it will respond to all commands in the order that they are received.

5.3 OVERLAP

The OVLAP function is used to make a visual comparison between two spectra by superimposing a corresponding half or quarter memory over the currently displayed section of memory. Note that the function cannot be enabled if the MEMORY switch is in the 1/1 position.

The corresponding memory sections are set forth in the table below:

Current display	Overlapped section
1/2	2/2
2/2	1/2
1/4	3/4
2/4	4/4
3/4	1/4
4/4	2/4

The operator can modify the first half of the OVLAP dialogue to display another overlapped section of corresponding size simply by entering the desired number by way of the X Register. The second half of the dialogue is always the memory section currently being displayed.

The overlapped data is always displayed offset by 20% of the selected VERTICAL RANGE.

When the dialogue has been completed, pressing YES (in answer to OK?) will terminate the dialogue; the overlapped memory section will remain on the screen until the function is turned off by pressing OVLAP again.

After the Overlap dialogue has been completed, the MEMORY switch can be changed between halves or between quarters. This will allow other memory segments to be compared with the overlapped segment.

Note that if the MEMORY switch is changed outside of the original size memory segments, the function will turn itself off.

5.4 TRANSFER

The XFER function allows the operator to copy data from one memory segment to another. Enabling XFER simultaneously enables OVLAP and displays the corresponding memory segment, as listed in section 5.8 OVERLAP, above. If the default parameters are acceptable, pressing YES will copy the data in the upper, overlapped, segment to the lower, current, segment.

The default parameters are alterable through the X Register to allow the overlapped memory segment to be changed to a segment other than the corresponding segment. The only restrictions are that the segment being transferred to must be chosen by the MEMORY switch and that the transfer can only take place between segments of the same size.

Note that Energy Calibration equations are transferred with the data but ROIs are not.

5.5 PRESET

Each mode of data acquisition has its own default preset which can be changed as desired by the operator.

5.5.1 PHA Preset

The Series 40 provides several preset conditions for the termination of PHA data acquisition:

1. Live or true time.
2. Counts in a specific channel.
3. Total Integral of a specific Region of Interest.
4. Total net Area of a specific Region of Interest.
5. User defined with the Model 4241 Define/Use option. (Section 7.1.9 covers the user defined preset.)

Enabling PRESET brings up the following dialogue:

```
*TIME(L) TIME(T) COUNTS INT AREA USER VAL= 1000 SEC
X=                                   OK?
```

The default state of 1000 seconds of Live time is displayed and may be changed through the X Register.

Using NO to advance the * allows the choice of True time, any of the three computational presets or the user defined preset, which will bring up the question NEXT? in place of the question OK?

A response of YES (to NEXT?) changes the dialogue to allow the operator to enter, in the case of COUNTS, the desired number of counts and the specific channel that the analyzer is to monitor for that count level. The default parameters may be changed as usual through the X Register and the use of NO to advance the *.

When the * is at CHANNEL #, the current location of the cursor may be entered simply by pressing STORE.

If INTegral or AREA are chosen, the next line of dialogue will read

```
*INT (or AREA)  1000 COUNTS  ROI  FROM CH# 0 TO CH# 0
```

Enter the number of counts and press NO to advance the * to ROI. Pressing STORE will enter the limits of the current ROI. If the * is moved to FROM or TO, the ROI limits may be entered manually or by pressing STORE, which will enter the current cursor address.

Current ROI is defined at the end of Section 5.6.

It should be noted that, except in the case of Live time, acquisition does not stop exactly at the preset parameter. This is because Series 40 firmware prevents fraction of a second errors in the keeping of Live time. When the analyzer reaches preset, collection will stop at the next tick of the Live time clock.

A high Dead Time could cause a long real time to elapse before the next tick of the Live Time clock. In this case, Collect may be aborted by disconnecting the signal cable or by performing a Power Reset (section 2.2).

5.5.2 MCS Preset

If MCSS or MCSR has been enabled, the PRESET dialogue will show:

```
DWELL (N*10↑M USEC) N= 1 M= 2     SWEEPS = 1 (for MCSS)
                                  or SWEEPS = 0 (for MCSR)
```

The formula in parenthesis is read as "N" times 10 to the "M" power microseconds. The default preset, then, is set for 100 microseconds dwell time per channel.

The default state can be changed by way of the X Register and NO to advance the *, subject to the following rules:

1. "N" can be set for 1 through 15.
2. When "M" is set to 9, the dwell will be expressed as "N" minutes.
3. When "M" is set to 10, the dwell will be expressed as "N" hours
4. When "M" is set to 11, the dwell will be set to "N" times 10 minutes.
5. When "M" is set to 15, the channel advance, and thus the dwell time per channel, will be under EXTernal control.
6. Setting the preset to EXTernal will cause the firmware to count "N" External pulses before executing a channel advance.

The sweeps preset cannot be altered in the MCSS mode, but in the MCSR mode, the number of sweeps may be preset for the required number through the X Register. If the default parameter of zero is retained, the analyzer will interpret this as infinity. That is, the analyzer will continue to sweep through the memory until stopped manually or remotely. See section 4.16, Collect, for the two methods of MCS termination.

Note: in MCSR, the number of sweeps performed may, under some conditions, exceed the preset slightly.

5.6 REGION OF INTEREST

The Series 40 has provision for entering Regions of Interest (ROIs) to mark significant peaks in the spectrum for later analysis and readout. To enter an ROI, simply

position the cursor at one limit of a peak with the Scan control, press ENT ROI, and Scan the cursor to the other limit of the peak.

Each data point that the cursor passes through while ENT ROI is enabled will be intensified to indicate the data that is within the ROI. When the further limit of the desired ROI is reached, release the Scan button and press ENT ROI once again to disable the function.

1. ENT ROI always causes the region through which the cursor passes to be set to the ROI state.
2. CLEAR ALL clears all ROIs from the displayed memory section.
3. CLEAR ONE, if the cursor is not located within a ROI, clears the current ROI.
4. CLEAR ONE, if the cursor is located within an ROI, clears those channels within the ROI that are to the right of the cursor, as well as the channel containing the cursor.
5. In clearing any ROI, the data remains unaffected. Only the intensified region is cleared from the memory.

Current ROI is defined as the ROI in which the cursor is located, or if the cursor is not in an ROI, the ROI immediately to the right of the cursor.

5.7 EXPAND MODE

For a detailed visual analysis of the peaks within a spectrum, the Series 40 provides a variable horizontal expansion of the display.

Enabling EXPAND will cause the displayed data to change from the full display to an expanded portion of the display, 128 channels wide. The cursor will be located at the 25% point of the expanded window. That is, 32 channels of the window will be to the left of the cursor and 95 channels will be to its right.

Note that if the cursor is within 33 channels of the left end or within 95 channels of the right end of the normal display, it will not be placed at the 25% point of the window. It will remain in its original position.

In order to examine peaks of interest that may fall outside of the window, the Series 40 allows the size of the window to be multiplied by a factor of two. Pressing the "X" button on the keypad will double the number of channels in the window, expanded around the cursor. The cursor's location will not change: it will remain in the same channel and will still be at the 25% point of the multiplied window.

Each time the "X" button is pressed, the window size will be doubled again, up to a maximum of one-half of the selected normal memory region, but no more than 4224 channels.

To decrease the multiplied window, press the "÷" button on the keypad. This will divide by two the number of channels in the window, down to a minimum of 128 channels.

5.8 ROLL

When enabled, ROLL allows the Expanded 128 channel window to be moved through the spectrum by means of the Scan controls. Scanning the Expanded window will cause the data channels to appear to move in the opposite direction from the direction of scan while the cursor remains in place.

Since the function is dependent on EXPAND, enabling the function automatically enables EXPAND if it is not already enabled. Similarly, disabling EXPAND will automatically disable ROLL.

5.9 INTEGRAL

The INTEGral function will sum all of the data points in:

1. The current ROI, if ROIs are entered.
2. The entire memory segment displayed if no ROIs are entered.

5.10 CURSOR CONTROL

At the bottom center of the keyboard is the outline of a double headed arrow. The buttons within the arrow control the cursor.

1. The round buttons at either end of the arrow control cursor movement (Scan): one scans the cursor to the right and the other scans the cursor to the left.
2. Momentary operation of Scan will move the cursor one channel. Holding the scan button down will cause continous movement of the cursor at an accelerating rate.
3. Continous operation of Scan will disable the Keyboard. No other Pushbuttons will respond to the operator's touch until the Scan control is released. This is also true for all pushbuttons.

5.11 Index

The INDEX function is used to quickly move the cursor from one ROI to another; it operates according to the following rules:

1. If the cursor is in an unintensified portion of memory, INDEX will move the cursor to the left limit of the next ROI to the right of the present cursor position.
2. If the cursor is within an ROI, INDEX will move the cursor to the left limit of the next ROI to the right of the present cursor position.
3. If the cursor is at the left limit of an ROI, INDEX will move the cursor to the left limit of the next ROI to the right of the present ROI.
4. INDEX will "wrap around" memory: that is, the cursor may be moved from last ROI in the display to the first simply by INDEXing.
5. If EXPAND is enabled, INDEX will move the cursor to the left limit of the next ROI (if any) and place the cursor at the 25% point of the display.

5.12 HOME

When HOME is pressed, it moves the cursor to the left end of the display: either the memory section being displayed or the expanded display if EXPAND is enabled.

This feature can be used to move the cursor quickly to channel 0 to check the elapsed Live time or to Scan the cursor to the left "around the corner" to arrive at a data region at the upper (right) end of the display without scanning through the entire memory.

5.13 ENERGY CALIBRATION

The Series 40 has the capability of calibrating the displayed spectrum in energy units. The cursor location and the limits of any entered ROIs will then be shown in those units instead of as a channel address. Using this displayed energy information, an unknown radioisotope can be identified. The Series 40 will accept up to 7 Energy Calibration equations, one for Full memory, one for each Half and one for each Quarter of memory.

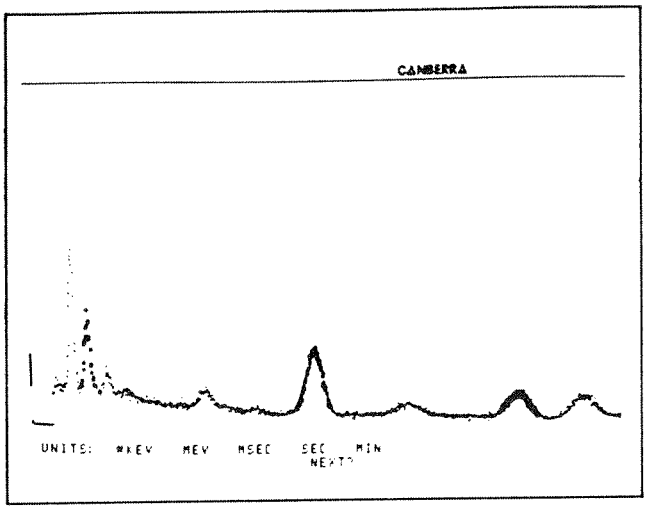


Figure 5-2
Initial Energy Calibrate

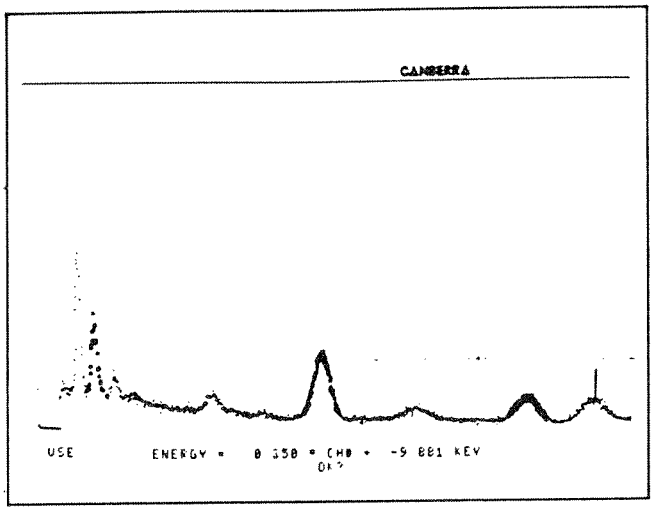


Figure 5-4
The High Energy Peak (1332.5 keV) has been Entered. Yes has been Pressed to Reveal the Calculated Energy per Channel (0.350 keV/Ch) plus the Offset Term (09.881 keV).

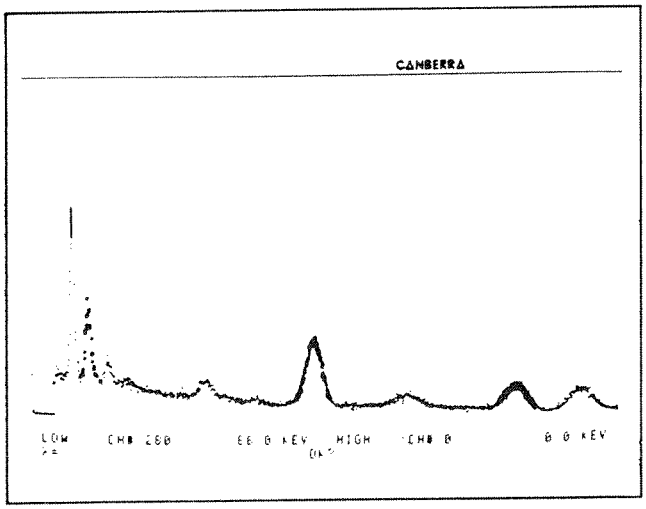


Figure 5-3
Lower Energy Peak (88.0 keV at Channel 280) Entered. The * is at the High Channel Number for Entry of the High Energy Peak.

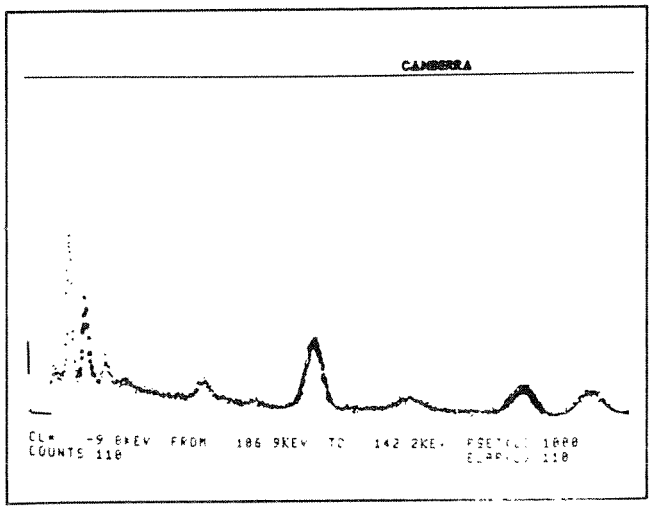


Figure 5-5
Yes has been Pressed again to Show the First ROI s Limits as Energy Units and Channel 0 as the Offset Term.

In addition to the energy units EV, KEV and MEV, the Series 40 offers the time units MSEC, SEC and MIN for calibration of Multichannel Scaling. The procedure is the same as for Energy Calibration.

The method uses a first order (straight line) calibration and is accomplished by answering the questions in the ECAL dialogue.

1. Press ECAL on the Keyboard to start the dialogue.
2. Advance the * to the desired calibration unit.
3. Press YES to advance to the parameter dialogue.
4. Enter the LOW channel either as a channel number or by pressing STORE to enter the current cursor location.
5. Press NO to advance the * in order to enter the Low energy.
6. Enter the energy into the X Register and press STORE.
7. Advance the * to HIGH and enter the channel and energy as in steps 4, 5, and 6.
8. Answer Yes (to OK?) to display the ECAL equation.

The Energy Calibration equation, showing the amount of energy (or time) calculated per channel, will be displayed for inspection until YES is pressed once more to terminate the dialogue.

It may happen that one of the limits entered is too large a value to be displayed. In which case the analyzer will display a series of "greater than" signs in place of the value. The memory will retain the entered value, however, and lower energies will be displayed correctly.

5.14 STRIP

The STRIP function allows the operator to subtract a factor-specified part of one spectrum, the reference, from another spectrum of the same size, the sample.

Before enabling the function, use the MEMORY switch to display the sample spectrum.

Press STRIP, which also enables OVLAP, to display the reference spectrum above above the sample spectrum. The overlapped memory segment will be the one corresponding to the setting of the MEMORY switch as listed in Section 5.3, OVLAP.

If the overlapped memory segment is not the desired segment, use the X Register to change the first part of the displayed dialogue.

STRIP *Q#1 OVER Q#3 F = 1.00

The factor (F) shown will either be the last computed RATIO, if one was computed, the last factor entered or the default parameter of 1.00. It, too, can be changed by advancing the * by way of NO and entering another factor through the X Register.

5.15 SPECTRUM NORMALIZATION

Normalization of a spectrum may be performed by stripping a region from itself using a negative Factor. The procedure is:

1. Transfer the spectrum to another memory segment.
2. Strip the spectrum from itself using a negative Factor.
3. Strip the original spectrum from the Normalized spectrum again, using a Factor of +1.00.

The last step is necessary because the Normalized spectrum is added to the original spectrum, resulting in a larger than desired amount of data in the Normalized spectrum.

An an example, transfer data from Q#1 to Q#3; Strip Q#3 from Q#1 using a Factor of -10.00; Strip Q#3 from Q#1 using a factor of + 1.00. The resulting Normalized spectrum will have an integral that is 10 times the integral of the original spectrum (Q#3).

5.16 RATIO COMPUTATION

The RATIO function provides a means of measuring the mathematical relationship between two elements of a spectrum. The ratios which may be measured are:

1. If INTEGral is enabled, the operator may compute the ratio Integral of a Region : Integral of a Region.
2. If AREA is enabled, the operator may compute the ratio Area of a Region : Area of Region.
3. If neither is enabled, the operator may compute the ratio Counts in a Channel : Counts in a Channel.
4. If both INTEGral and AREA are enabled, the calculation will be performed on AREA.

Note that since Live time and True time are stored in channels 0 and 1, ratio method number three may be used for measuring either the Live time or the True time relationship between two spectra.

Assuming that an Integral ratio is to be determined:

1. Press INTEGral
2. Press INDEX to advance the cursor to the first of the two ROIs between which the ratio is to be determined.
3. Press RATIO. Note that the Ratio, displayed at the lower right corner of the CRT, equals one.
4. Press INDEX to advance the cursor to the second ROI of the two between which the Ratio is to be determined.
5. Note that a marker cursor remains at the first ROI to indicate which ROI is the basis of the ratio computation.
6. The ratio computation between the two ROI Integrals is made automatically and the result is displayed as a new value of Ratio.

To compute the ratio of the Areas of two ROIs, the same method is used, but with AREA enabled instead of INTEGral.

To compute the ratio of the counts in two channels, both AREA and INTEGral must be disabled [illegible] cursor placed in the first of the two channels, RATIO [illegible] the cursor scanned to the second of the two channels. Note the RATIO being updated as the cursor is scanned through the memory.

Alternatively, if the two channels are not adjacent, they may have an ROI of one channel each entered in them and the cursor may be Indexed between the two one-channel ROIs.

The Ratio function may also be used in Overlap. Enable RATIO in the third quarter (for instance) with the cursor in the desired channel, change the MEMORY switch to 1/4 (for instance) and enable OVLAP (section 5.3). The marker will be visible in the overlapped display; the cursor in the lower part of the display can be moved to a channel of interest for a Ratio comparison.

5.17 AREA

The AREA function computes the number of counts in a peak that are above the background level. The method of computation of background level and of area are given in Appendix D.

To calculate peak net Area, enter an ROI around the peak of interest and press AREA. The function will also enter histogram bars: vertical intensified lines from the baseline to the data point in each channel in the ROI.

If the cursor is not in an ROI, the function will calculate the Area of the next ROI to the right of the cursor.

If no ROIs are entered, the function will calculate the Area of the displayed memory segment but will not enter any histogram bars.

Section 6. Input/Output

When the operator requires that data be stored on or retreived from an external device, the two functions READ IN and READ OUT will be used. This section covers the use of these two functions.

6.1 DATA READOUT

The READ OUT pushbutton allows the operator to transfer data from the Series 40's memory to a peripheral recording device. When first enabled, the function offers the following dialogue:

```
DEV=  TTY  *EIA  (see notes)  TAG = 0
X=                 OK?
```

The default state readout device is either EIA or CAS (see note 1). By moving the *, the operator may choose to read data out to any other available peripheral device.

The last item in this line of dialogue allows the operator to set a Tag Number for identifying a particular readout; its use is not necessary to obtain a readout. In successive readouts, the Tag Number will automatically be incremented by one with each readout.

Note[1]: CAS may be replaced by EIA, depending on the position of an internal control switch. See Appendix A 5 for information on changing the switch position.

Note[2]: The device codes X-Y, SER, GRA, or MT will appear in addition to the above listed codes if the Models 4251, 4252, 4253, or 4254 are present in the analyzer.

- TTY: Selects Teletype (current-loop) readout. Automatically sets the correct baud (data transfer) rate for the Teletype.
- CAS: Selects Cassette readout. Sets the baud rate (1200) and leader generation for the Model 5421 Digital Cassette.
- EIA: Selects EIA (RS-232) device readout. Mutually exclusive with CAS.
- X-Y: Selects X-Y Plotter readout. Requires Model 4251.
- LPT/PLT: Selects printer/plotter readout. Requires Model 4252.
- GRA: Selects Graphics Plotter readout. Requires Model 4253.
- MT: Selects Magnetic Tape readout. Requires Model 4254.

Models 4251, 4252, and 4253 are mutually exclusive.

With some I/O devices, pressing YES will start the readout. With others, answering YES to the question OK? will bring up the next line of the dialogue:

```
MEM + MODE  *ROI + ASCII  FULL + ASCII  ROI BRIEF  FULL + BINARY
                          OK?
```

MEMory plus MODE refers to the choices on the remainder of the line: memory choice and readout mode choice.

The modes offered are different data transfer codes. Most peripheral devices can recognize only one mode; the instructions for each device will specify which mode is to be used.

- MEM: FULL will read out all of the data in the memory segment chosen by the position of the MEMORY switch.

  ROI will read out the Live and True time and the data in all Regions of Interest in the selected segment of memory.

- MODE: ASCII puts the read out data in a format suitable for a current-loop (Teletype) terminal. BINARY puts the read out data in a format suitable for Magnetic Tape or Cassette Recorder.

ROI BRIEF will provide an ASCII readout of ROI summaries without the raw data.

If the wrong mode is chosen for the peripheral device being used, the data read out will be unintelligible.

6.2 CASSETTE RECORDER I/O

The Cassette Recorder provides a convenient low cost means of storing spectra collected with the Series 40. This section describes the operating procedures for storing and retrieving (reading out and reading in) data using the Cassette Recorder. It will accept data in either the ASCII mode or the binary mode. The binary mode is normally used because ASCII characters use more tape space and take more time to transmit.

Connect the Model 5411, using its built-in cable, to J101 (EIA) on the Series 40's rear panel and connect the Cassette's line cord to a source of ac power. Be certain that the Read Out menu offers CAS; if EIA appears, an internal switch must be changed (see Appendix A.5).

Connect the Model 5421 to its Interface Module and the Module to J101 (EIA) on the Series 40's rear panel.

Recording data with the Cassette Recorder:

1. Insert a blank cassette in the Recorder.
2. Rewind the cassette to its beginning with the REV/REW button.
3. Reset the Recorder's counter to zero by pressing the button next to the counter.
4. Simultaneously depress the PLAY and RECord buttons.
5. Press READ OUT on the Series 40's Control Panel.
6. Select CAS and Press YES on the Keyboard.
7. Select Full Memory and Binary Mode (FULL + BINARY).
8. Press YES on the Keyboard to start the readout. Note the buzzing sound that starts a few seconds after the tape starts moving. This indicates that data transfer is taking place.
9. Series 35, Series 40, Series 80, and Series 85 recorded data are mutually compatible if the FULL + BINARY mode is used on the Series 40.
10. Series 30 data can be read in to the Series 40.

After the readout is finished, wait a few seconds for tape motion to stop. When the tape has stopped, record the number shown on the digital counter. This will be the spectrum indentification number associated with the next spectrum recorded. To record another spectrum, repeat the procedure listed above, starting with step 4.

6.3 PLAYBACK OF DATA

1. Insert the cassette containing the desired data into the recorder.
2. Rewind the cassette to its beginning with the REV/REW button.
3. Reset the recorder's digital counter to zero by pressing the button next to the counter's readout.
4. Using the CUE/FFWD button on the recorder, search the tape until the desired spectrum identification number is displayed on the digital counter. If the number is overshot, use REV/REW to back up the tape as needed. Note that positioning of the tape is not critical: ± 1 digit is adequate.
5. Press the PLAY button.
6. Press the READ IN button on the Series 40's Control Panel.
7. Select CAS and press YES on the Keyboard to start read in.

As in readout, the recorder will "buzz" indicating that data transfer is taking place. Tag number, ID and ECAL equation, as well as data can be read in.

6.4 TELETYPE I/O

In addition to the EIA/Cassette interface, the Series 40 also includes a standard Teletype (current-loop) interface. This section describes using this interface with the Canberra Model 5107 series Teletype.

Connect the Teletype to J102 (TTY) on the rear panel of the Series 40. Apply ac power to the Teletype and move its front panel mode switch to the LINE position.

1. Press READ OUT on the Series 40's Control Panel.
2. Select TTY and press YES on the Keyboard.
3. Select either FULL memory or ROI plus ASCII mode.
4. If a punched paper tape is desired, turn the TTY's punch ON.
5. Press YES on the keyboard to start the readout.

The results of a FULL + ASCII readout on a Teletype are shown in figure 6.1.
The results of a ROI + ASCII readout are shown in figure 6.2.
The results of an energy calibrated ROI + ASCII readout are shown in figure 6.3.

An ASCII encoded paper tape is mutually compatible with the Series 35, Series 40, Series 80, and Series 85. A paper tape made by a Series 30 can be read into the Series 40.

6.5 ALPHANUMERIC DATA ID

As an aid in identifying the data recorded in a given readout, the Series 40 provides a means of entering an alphanumeric identification (ID) label of up to 23 characters.

To enter an alphanumeric ID label with a current-loop device (TTY):

1. Set the MEMORY switch to the desired position.
2. Press READIN.
3. Press YES to activate the terminal keyboard.
4. On the terminal keyboard type:
   a. CTRL/B (hold down CTRL and press the letter B).
   b. Any alphanumeric label of up to 23 characters.
   c. CTRL/D (hold down CTRL and press the letter D).
5. When the CTRL/D is received, Readin will terminate. Press READ OUT to display the label.

This ID label will be read out with all data from the Analyzer and read in with all data from an external recording device.

Houston Plotter Calibration:

To assure coincidence between the Analyzer's full scale plot signal and the Plotter's full scale plot, it may be necessary to calibrate the Houston 2000CZ Plotter:

1. Clear the Analyzer's memory and press READ OUT.
2. Place the switch on the Y module (the right-hand side of the Plotter's front panel) to FULL SCALE.
3. Adjust the X and Y F.S. ADJ. pots (not the X Expanded FS Adjust pot), so that the beam pointer is at 15 on the X scale and 10 on the Y scale.
4. Place the switch on the Y module at ZERO.
5. Adjust the X and Y ZERO pots (not the X Expanded Zero pot) so that the beam pointers are at zero on both axes.
6. Repeat steps 2 through 5 until steps 3 and 5 show no change.

Note: the Expand function on the Plotter, which has no relation to the Analyzer's Expand function, is not used with the Series 40.

6.7.3 Specifications and Signals

Data can be recorded in either log or linear format in the line plot or point plot mode on X-Y or T-Y plotters.

A. Specifications:

Signal Amplitude	0 to + 5 V.
Resolution	1 part in 1024 (10 bits).
Output Impedance	≈ 93 ohms.
Integral Nonlinearity	< ± 0.1% of full scale per °C.
Zero Drift	< ± 0.01% of full scale per °C.
Gain Drift	< ± 0.02% of full scale per °C.
Internal Rate Control (RV1)	Adjustable from 2 to > 10 channels/sec. Factory set at 2 per second.
External Rate Control	Must exceed internally set rate. Maximum advance rate is > 100 per sec.

B. Connector Signals:
J107 (or J108), 25-pin connector

PIN	SIGNAL	DESCRIPTION
23	PLTX	0 to + 5 V analog signal.
2	XGND	Ground.
21	PLTY	0 to + 5 V analog signal.
4	YGND	Ground.
5	SEEK	Nominal 100 μsec output pulse when plot signals are changed; TTL compatible; positive true polarity is standard; internal jumper plug (D-E) inverts polarity.
6	CPC	Completed plot input from plotter; ac coupled; advances on negative going edge; minimum excursion = 4 V; rise time < 0.5 μsec.
9	NABL	Plotter enable output; TTL compatible; negative true polarity is standard; internal jumper plug (B-A) inverts polarity.
14	GND	Ground.

6.7.4 Hewlett-Packard Plotter Cable Connections

The Hewlett-Packard 7004 Plotter uses a Canberra-supplied interconnecting cable. The cable pin-out is:

HP 25-PIN connector	Series 40 J107 (J108)	Signal
1	21	PLTY
2	4	YGND
6	14	Ground
14	23	PLTX
15	2	XGND
HP 9-pin connector		
2	5	SEEK
3	14	Ground
4	6	CPC
5	9	NABL

6.7.5 Model 4251C General Purpose X-Y Plotter Cable

25-pin Connector	Wire Color	Plug Color	Signal
21	Red	Red	PLTY
4	Orange	Black	YGND
23	Blue	Red	PLTX
2	Green	Black	XGND
14	Black	Black	Ground

6.8 MODEL 4253 GRAPHICS PLOTTER

The Model 4253 Graphics Plotter Interface can be used with the Hewlett-Packard HP 7470A (Canberra Model 5207A) two-color Graphics Plotter. It can also be used with the HP 7225, with 17603 Personality Module and the HP 7220 Plotters (former Canberra Models 5207 and 5206).

6.8.1 Plotter Setup

The Plotter's rear panel has an 8-pole rocker switch:

Pole	Setting
S2	0
S1	0
D/Y	1
A4/US	1
B4	1
B3	0
B2	0
B1	0

Refer to the HP operator's manual for the meaning of these switches and for specific instructions on plotter setup.

The cable supplied with the Plotter Interface is marked "EIA" or "MCA" at one end and "PLOTTER" at the other end. Connect the Interface cable to J107 (or J108) on the Analyzer and to the Plotter at:

7220 Modem Connector
7225 Signal Interface Connector
7470A EIA Connector

Another cable is provided with the 7220 for a self-test function; see the Plotter's Operating Instructions for its use.

6.8.2 Plotter Operation

The Series 40 should be turned on before the Plotter is turned on to assure proper Plotter operation.

With the Plotter set up, the cable connected and the paper loaded, press READ OUT on the Series 40 and select GRA as the readout device, then press YES to start the readout.

The Plotter will read out the alphanumerics and the spectrum currently displayed. The MEMORY switch and INTEG, AREA, ECAL, USE, and RATIO, if desired, must be selected before starting the readout.

Figure 6-5 shows a typical Graphics Plotter readout.

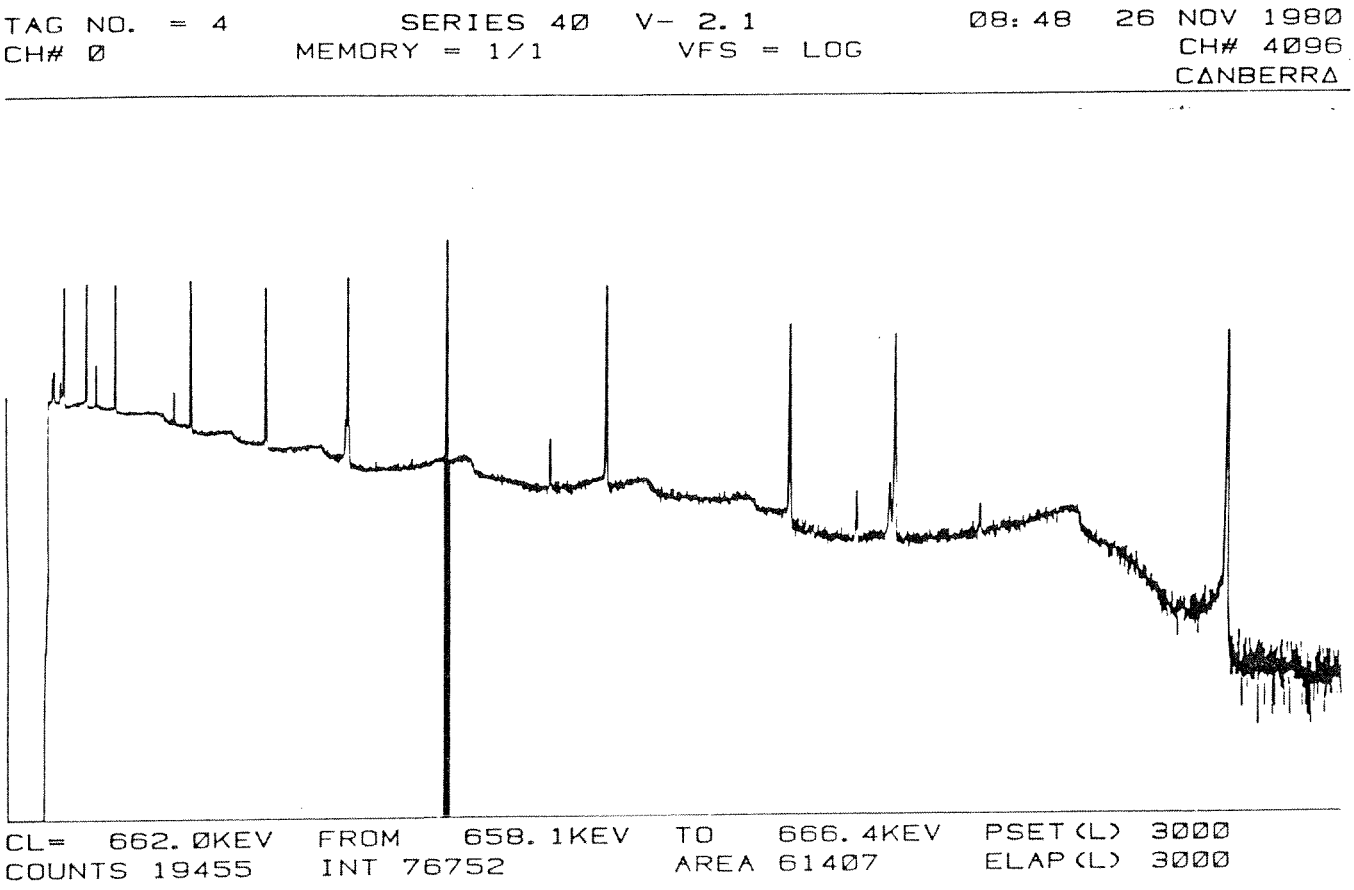

TAG NO. = 4
SERIES 40 V- 2.1
08:48 26 NOV 1980
CH# 0
MEMORY = 1/1
VFS = LOG
CH# 4096
CANBERRA
CL= 662.0KEV FROM 658.1KEV TO 666.4KEV PSET (L) 3000
COUNTS 19455 INT 76752 AREA 61407 ELAP (L) 3000

Figure 6-5
Typical Graphics Plot

Section 7.
Analysis Options

7.1 MODEL 4241 DEFINE/USE

The Define/Use option allows the operator to enter, either manually or from an external device, up to four algebraic equations. The equations may use one or two Constants and one or two Variables plus Live time (TL). All operations are performed in Floating Point arithmetic.

1. Parenthetical nesting is provided up to four levels.
2. An equation may be a maximum of 57 displayed characters. Note that some operations require more than one character: Square Root, for instance, is displayed as SQRT: a total of 4 characters of the 57 available.
3. Computation is performed according to the hierarchy of operations shown in the following list. Within a given level, computation is performed from left to right.

Operation	Hierarchy
√ (SQRT) e^x (EXP) Unary minus (-)	First level
Multiplication (*) Division (/)	Second level
Add (+) Subtract (-)	Third level

4. In addition to the usual operators, the Series 40 provides exponential notation to the base *e* (natural logarithm), as well as to the base 10. The EEX key on the keypad is used for both bases.

   The Firmware picks which base to use by the following rules:

   A. If a numeric entry precedes the EEX, the Firmware will use the base 10. That is, an entry of 4.7, EEX, 4 will be read as 4.7 x 10^4. It will be displayed as 4.7E4.
   B. If there is no number preceding the EEX, the Firmware will use the base *e*. That is, an entry of 5, x, EEX, 3 will be read as 5 times e^3. It will be displayed as 5 x EXP3.

   Note that the exponential notation on the display varies with each base: when the base ten is raised to a power, the display shows "E"; when the base e is raised to a power, the display shows "EXP".

5. Constants may be defined for each equation as K1 or K2 or entered as numeric literals in integer, fixed decimal or exponential format. Constants are always displayed exponentially; base e cannot be used.

7.1.1 Editing

As the equation is entered, a mistaken entry can be deleted by pressing NO, which will delete the most recent entry. If the mistake is several entries back in the equation, it may be deleted by pressing NO several times which will erase each remaining entry at the end of the equation. When the mistake has been deleted, the correct entry can be made and the equation continued. In addition, the entire equation may be erased by pressing the Clear (CLR) key.

7.1.2 Define

Pressing the DEFINE button reveals:

```
EQU#1
X=
                    OK?
```

The default equation number (1) may be changed to 2, 3, or 4 by way of the X Register. Pressing YES will show the next line of dialogue:

```
*DEFINE  LOAD
                    OK?
```

LOAD allows the operator to Load a previously defined equation which has been stored externally. If LOAD is selected, the operator may select TTY (Teletype) or CASsette as the device to Load from. A Response of YES starts the Load readin.

Accepting DEFINE with a YES shows:

```
EQU#1
X=
                    OK?
```

The X Register is used to enter the desired equation. When the equation is complete, press STORE to transfer the equation to memory.

When the equation has been entered in memory (with STORE), press YES to bring up the next line of dialogue:

```
*K1  0.00E00     K2  0.00E00
 X=
                    OK?
```

If either K1 or K2 was specified as part of the equation, they will be entered here. Press NO to advance the * to K2. If neither was specified as part of the equation, this section may be disregarded. In either case, pressing YES once more will reveal:

```
V1= CL  CNT@CH#  INT@ROI#  AREA@ROI#  EQUA#
 X=                    OK?
```

If Variable one (V1) was specified in the equation, it will be entered here. If not specified, press YES to go on to the *dialogue for variable two* (V2), which uses the same format.

A Variable is defined as:

1. CL: The current Cursor Location (channel number). If the spectrum is energy calibrated, energy units rather than a channel number will be used in the calculation.

2. CNT @ CH#: The count in a specified channel. A specific channel number may be entered, or STORE may be pressed to enter the channel number of the current cursor location. Entering channel zero as the channel number will be interpreted as counts in the current cursor channel.

3. INT @ ROI#: Integral of a specified ROI. Entering zero as the region number will be interpreted as the current ROI. See section 5.6, last paragraph, for the definition of current ROI. If more than one ROI has been entered, the ROIs are counted from left to right to signify which ROI # is being referred to.

4. AREA @ ROI#: Area of a specified ROI. ROI defined as in Step 3.

5. EQUA #: The current value of the specified equation. This function allows equations to be chained: if the current equation needs to have more than two Variables, the third, or greater, Variable can be defined in another equation and referred to with this function. Reference to the current equation number is not legal.

   When the two Variables have been entered, pressing YES will reveal:

   SAVE EQU # n
   OK?

The displayed equation number is the number of the current equation. NO will terminate the dialogue. YES will allow the choice of external device for saving the equation.

If DEFINE is pressed again after entering an equation, the same initial dialogue is displayed; after DEFINE is accepted with a YES, a new line of dialogue will be displayed:

USE OLD EQU # n
OK?

The current equation "n" will be displayed in the X Register. If it is to be retained, pressing YES will allow the dialogue for the equation to proceed. If NO is pressed, the current equation will be deleted from memory, allowing a new equation to be entered in its place. If DEFINE is disabled at this point the equation will no longer be available.

If YES is pressed, to USE OLD equation, the dialogue will go on to the Constant parameters that were entered for the equation so that they may be altered if desired. Pressing YES to accept the existing, or the altered, Constant parameters will allow the dialogue to proceed to the first of the Variable parameters for review as with the Constant parameters. Pressing YES again will bring up the second of the Variable parameters for review and pressing YES once more will show the SAVE dialogue.

7.1.3 Save

Once an equation has been entered in memory, it can be saved by reading it out to an external device, such as a Cassette or a Teletype's paper tape punch. The SAVE dialogue, which appears at the end of the Define dialogue, when answered with a YES, will reveal:

DEV= *TTY CAS

After selecting the appropriate readout device, press YES to start the readout. Pressing NO bypasses the SAVE operation, leaves the equation in memory and returns the display to normal.

7.1.4 Load

To enter an externally recorded equation into memory, the Load feature is used. The second line of the Define dialogue allows the choice of Learn or Load. Answering YES to LOAD will bring up:

DEV= *TTY CAS

After selecting the appropriate readin device, press YES to start the readin.

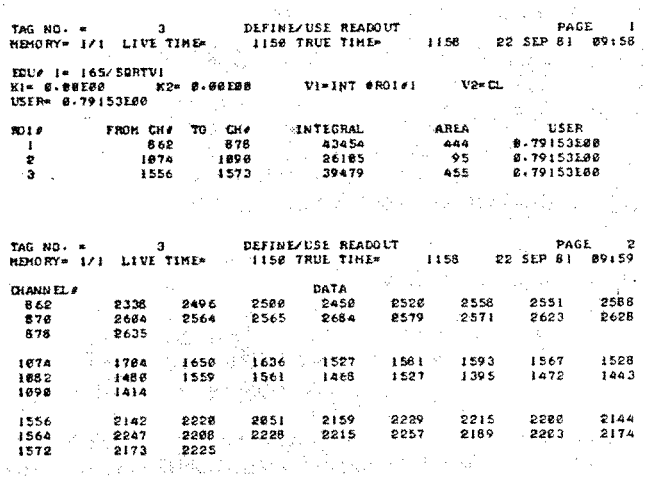


Figure 7-1
Readout Showing
Define/Use Equation

7.1.5 Use

Pressing the USE button will allow the choice of equation to be used; the number displayed is changeable through the X Register. Pressing YES will enable the selected equation. As data is accumulated in the analyzer, the equation will repeatedly be evaluated. The continually updated results of the ongoing evaluation will be displayed in the lower right corner of the screen, in place of the Preset, as USER=.

7.1.6 Accumulator

Define/Use also includes a floating point register that can be used as an accumulator (ACC) of instantaneous equation results. When USE is enabled, the Accumulator can be enabled by pressing STORE, which will allow the register to be used to keep a running total of the results of the equation's continual evaluation of the data. Mathematically, the Accumulator will perform ACC = ACC + VAL each time STORE is pressed, where VAL is the equation value currently displayed in the USER register. This feature can be used to sum the results of several equations or of several runs of one equation.

7.1.7 Read Out

If USE is enabled when a Read Out is started, the current equation will be printed in the Report Header, along with the values for the Constants and Variables for that equation. If ROI # n is specified, the results of the equation for that ROI will be printed in the Header. Figure 7.1 shows a typical Define/Use readout.

If the equation contains a reference to ROI # 0 (the current ROI) and the Read Out is a ROI type, the equation will be re-evaluated for each ROI and the equation's value will be included in the data summary for each ROI. See Section 5.6, third paragraph, for the definition of current ROI.

Note that if either of the Variables is not defined, it will be shown in the readout as V1 (or V2) = CL, the default state for the Variables.

7.1.8 An Example

One useful equation that might be entered is the one that defines the percent error (% ERR) of the integral of a given region. This equation will be used to show how a complex equation can be entered with the Define/Use option. The equation reads:

$$\%ERR = 165 \times (INT + ((N \div 2)^2(B_1 + B_2))) \; 1/2 \div (INT - ((N \div 2) \times (B_1 + B_2)))$$

Where N = the number of channels in the region being evaluated, B_1 = the number of counts in the last channel before the region, B_2 = the number of counts in the first channel after the region, INT = the integral value of the region.

To enter this equation in a form acceptable to the firmware, it must first be slightly altered to, and entered as:

$$K1 \times \sqrt{(V1+(K2 \times K2 \times V2))} \div (V1-(K2 \times V2))$$

Where K1 = 165, for a 90% confidence level,
V1 = Integral of the region,
K2 = (N ÷ 2),
V2 = (B_1 + B_2).

Since B_1 and B_2 are variables also and since the equation only allows for two variables, which have already been defined, they must be entered in a second equation. The second equation, EQU# 2, can be defined as V1 + V2, which will correspond to B_1 and B_2 of the first equation.

In entering K2, the evaluative feature of the X Register, mentioned in section 2.3.4, can be used. Enter the ROI's, Stop channel number minus Start channel number plus one, divide by 2 and STORE. For example, 419 - 342 + 1 ÷ 2 will be evaluated and stored as 39.

The accompanying figures illustrate the method of entering the two equations necessary for defining %ERR of an Area. Note that the firmware must convert the decimal entries to a digital form for manipulation and then convert back to decimal form for display. This process has an inherent error, however small, due to the truncation (rounding off) of entries in the conversion process. The displayed results of the evaluation are accurate to ±1 least significant digit.

Figures 7-2 through 7-14 illustrate defining and using this equation. Figures 7-15 and 7-16 illustrate the use of the Accumulator register.

7.1.9 User Preset

To use a defined equation as a Preset condition, press PRESET to see:

*TIME (L) TIME (T) COUNTS INT AREA USER VAL = n
X = OK?

The value displayed will be the last entered Preset. Advance the * to USER with the NO button and press YES to see:

*USER = n EQU # 1
OK?

The desired value for the Preset can be entered through the X Register while the * is at USER. Press NO to advance the * to EQU # to enter the appropriate Equation number for the Preset function to evaluate, then press YES to terminate the dialogue.

The Preset portion of the normal display will now show "PSET (U) = ". To display the evaluation of the equation as data acquistion proceeds, enable USE, Equation 1, which will change "PSET (U)=" to "USER =". It is not necessary to do this since the Preset function evaluation takes place automatically, but the operator may wish to observe the continuing evaluation of the equation.

Since the Preset is an increasing function, using the % Error equation will require a change in the equation because % Error is a decreasing function. Simply change the equation to "10-(equation)" and enter the Preset value as the difference between 10 and the desired value. For instance, if data acquisition is to stop when the % Error has decreased to 7%, enter the Preset value as 3, the difference between 10 and 7 (the desired value).

Enabling COLLECT will allow the acquisition to continue until the "ELAP (U)" equals 3. Note that the Elapsed value will start as a negative number, which will be displayed as a series of " > " signs, because the initial % Error value will be greater than 10. When the Elapsed value has increased to 3, acquisition will stop.

To demonstrate this function, enter the equation as defined in section 7.1.8, above. Enter Equation 3 as X = 10-V1, where V1 is defined as EQU # 1. In the User Preset dialogue, set the Preset value equal to 3 and refer to EQU 3. Proceed with data acquisition until the Preset (3) is reached and Collect is terminated. Enable USE with Equation # 1 and check that the USER = portion of the display does indeed equal less than 7, showing that the acquisition stopped when the % Error decreased to less than 7%.

Note that although this is a convenient method for demonstrating this function, it may not be successfully display both the equation's results and the elapsed preset while the analyzer is in active Collect. In actual use it is preferable to use the "10-equation" format and preset on that equation.

If a Preset is to be used that is not expressed as a percent but is a decreasing function, the Equation must be defined as "(10-equation) ÷ 100."

7.1.10 Operator's Equations

Use this space to make notes for your own equations.

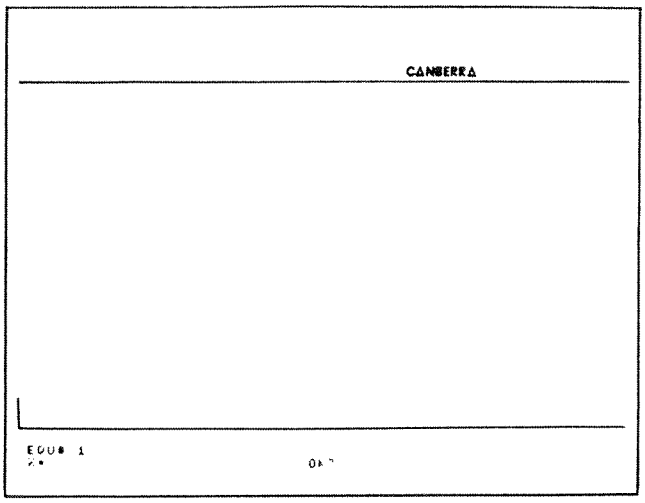


Figure 7-2
Define Enabled

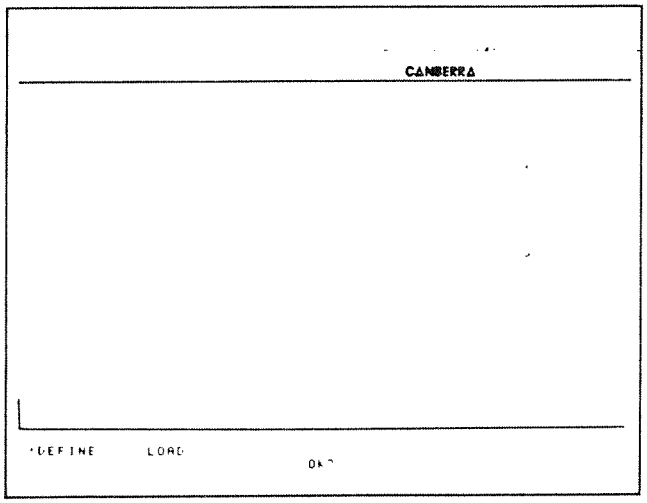


Figure 7-3
Yes Reveals Choice of Define or Load

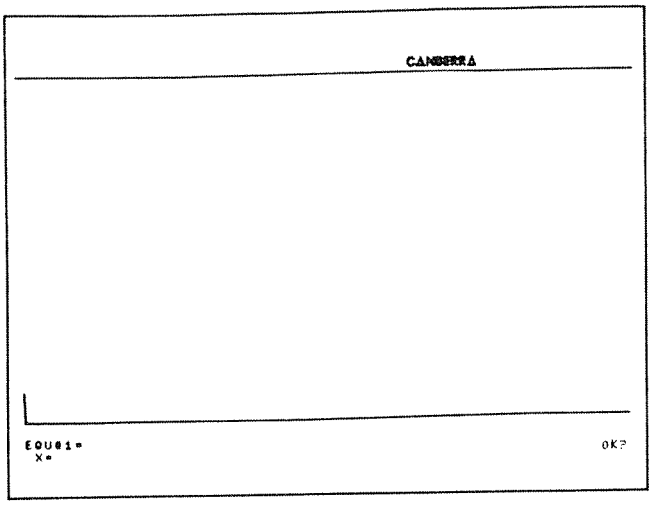


Figure 7-4
Yes Reveals the X Register

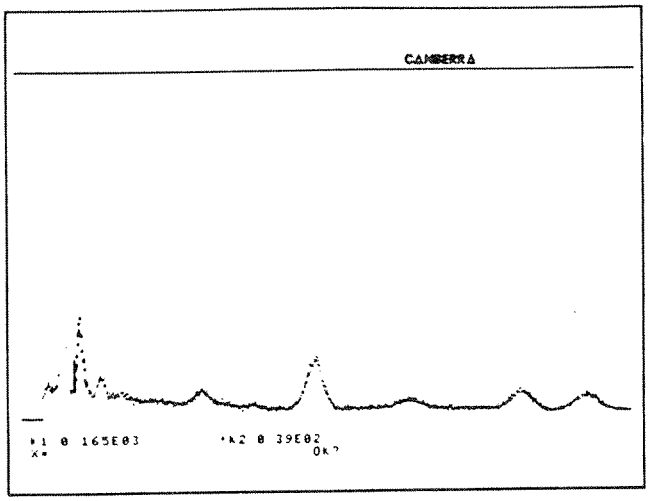


Figure 7-7
Yes Reveals the Dialogue for Entering Constants.
The Two Constants have been Entered.

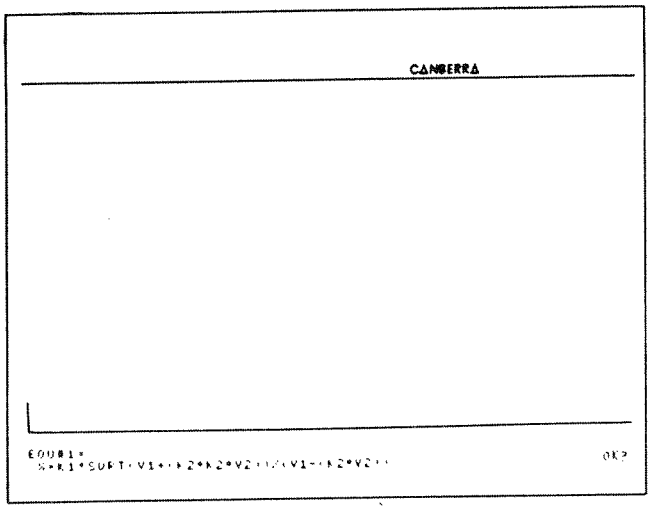


Figure 7-5
The % ERR Equation has been Entered in the X Register

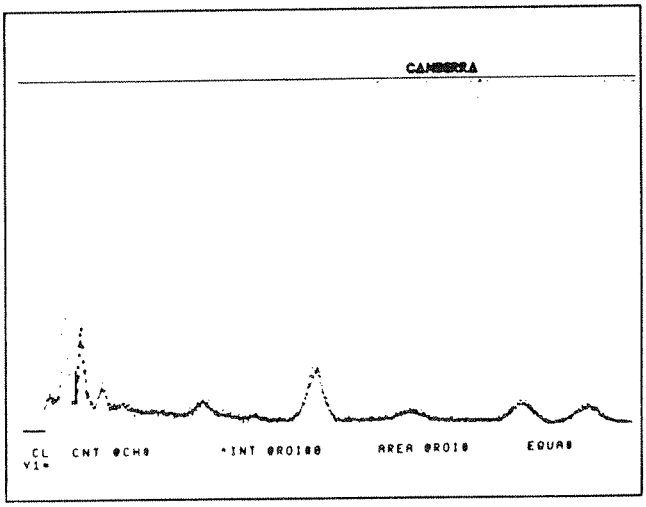


Figure 7-8
Yes Reveals the Variable Dialogue, which has been Set to the Integral of ROI #0 (the Current ROI).

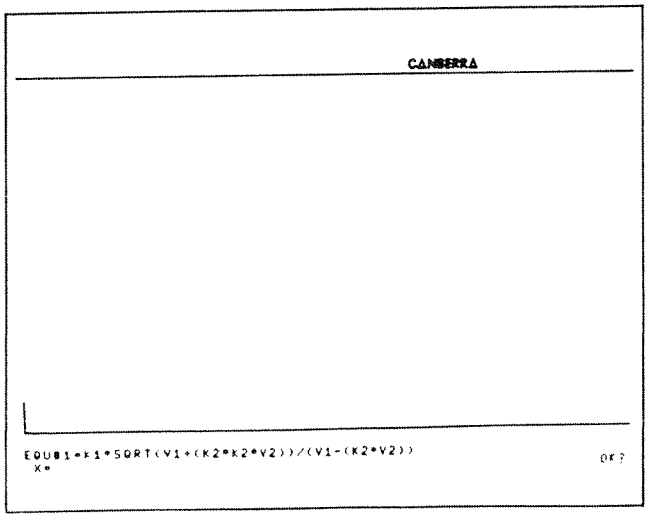


Figure 7-6
STORE Places the Equation in Memory

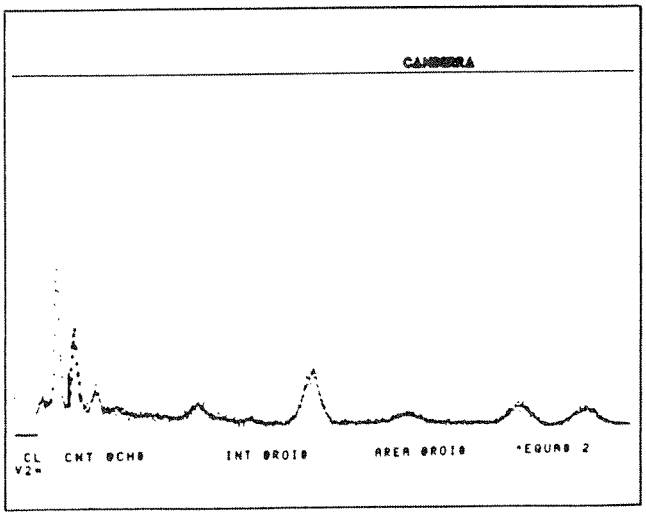


Figure 7-9
Yes Reveals the Second Variable, which has been Set to Equation # 2.

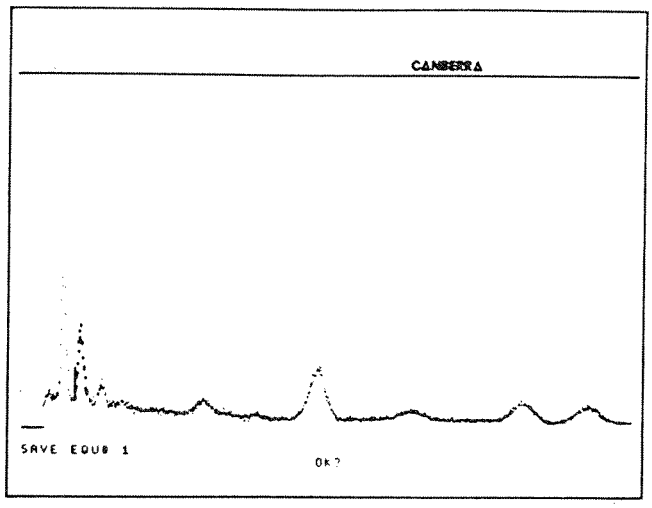


Figure 7-10
Yes Reveals the Save Dialogue. No was Pressed to End the Dialogue.

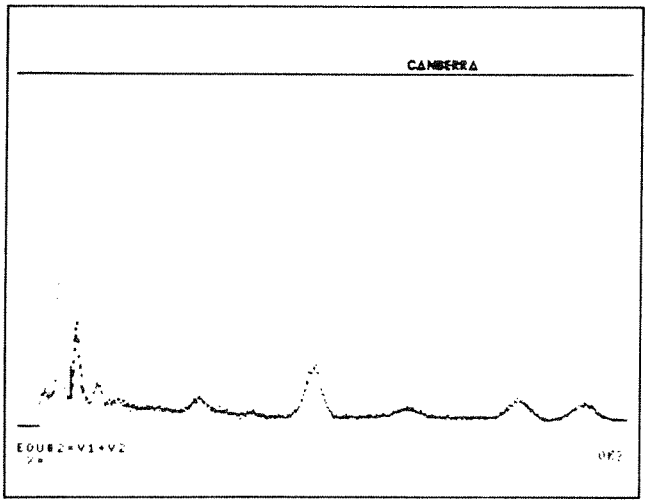


Figure 7-11
Define was Pressed to Enter Equation # 2 as V1 + V2.

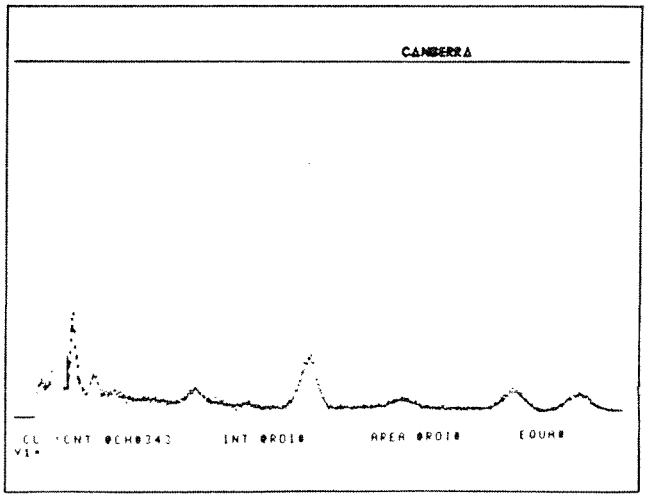


Figure 7-12
Variable 1 has been Entered as Counts in Channel 343, the last Channel before the ROI.

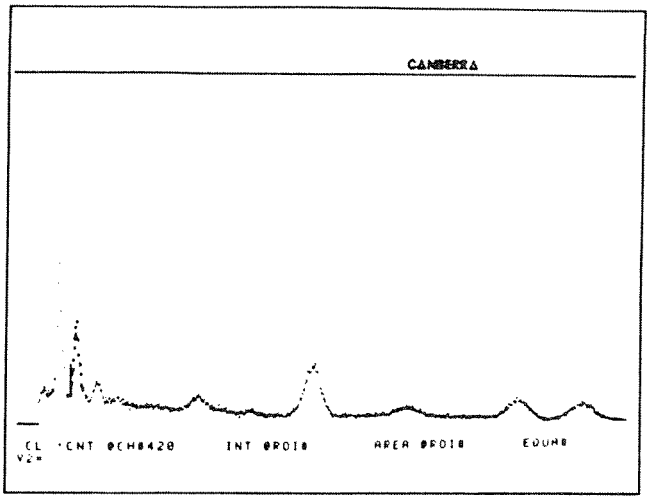


Figure 7-13
Variable 2 has been Entered as Counts in Channel 420, the first Channel after the ROI.

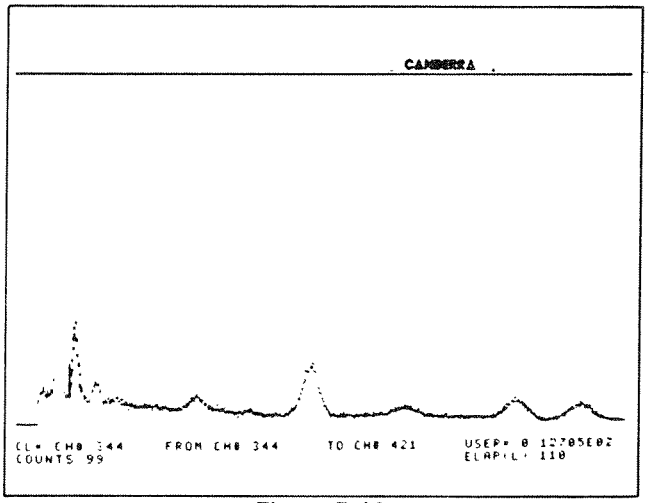


Figure 7-14
Equation 2 has been Completed. USE has been Enabled, showing the Results of the Equation's Evaluation in the User Register.

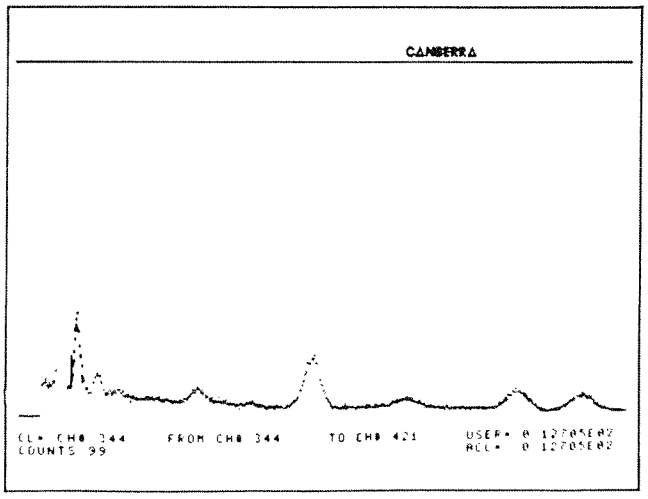


Figure 7-15
Store has been Pressed, Enabling the Accumulator. ACC equals USER Initially Because Collect is Inactive.

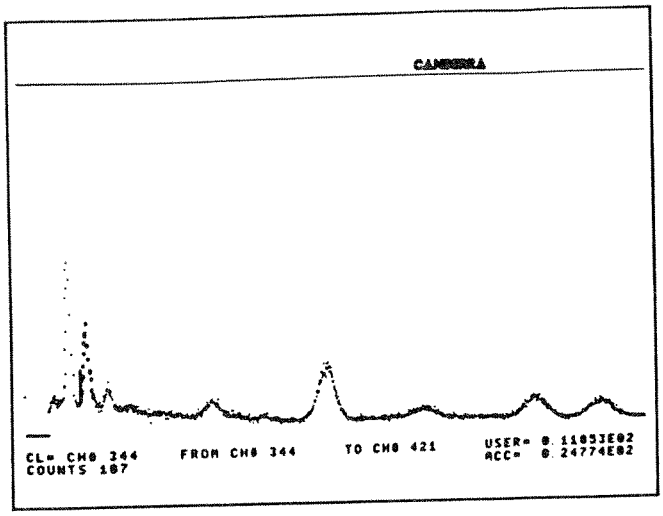


Figure 7-16
Further Data has been Acquired. Both User and Accumulator Registers have been Updated and are no Longer Equal.

7.1.11 The Ap-Pak

The Ap-Pak extends the capability of the Define/Use option by providing ten predefined functions, each of which will solve a common data analysis problem. These equations, numbered 5 and greater, are a permanent part of the Analyzer and will not be lost when power is turned off.

Note: if the Ap-Pak program is not in the Analyzer, requesting equation number 5 or greater will display "Illegal Entry".

Several of the equations must be completed by assigning values to the constants K1 and and K2. To assign the values, press DEFINE and store the equation's number (see Table 7.1). Then accept the equation (YES to USE OLD?) and enter the constants at K1= and K2=. Now press YES to see the SAVE dialogue (Section 7.1.3).

Any defined equation can be accessed by pressing USE:

```
*EQU#1
X=                OK?
```

Enter the Ap-Pak equation's number (5 or greater) through the X Register.

When YES is pressed the equation will be calculated. The results will be displayed at the lower right of the screen in place of USER=. Each equation has its own callout which appears instead of the USER callout. See Table 7.1.

Table 7.1
Ap-Pak Equations

Number	Name	Callout
5	Centroid	CENT
6	Full Width at Half Maximum	FWHM
7	Counts per second	CPS
8	Percent Error of an Area	% ERR
9	Percent Dead Time	% DT
10	part of equations 11 and 13	HLIF see note
11	Efficiency	EFFIC
12	Activity in μCuries	ACTIV see note
13	Decay Corrected Activity	DCACT see note
14	Dose Rate in mR/hr	DOSE see note

Note: equation 10 is used to enter the half life for equations 11 and 13. Equation 12 uses the results of equations 10 and 11. Equations 13 and 14 use the results of equations 10, 11, and 12.

Appendix F lists each of the equations in full.

7.1.12 Using the Ap-Pak Equations

Equations 5 through 9 are complete; no further entry is required. Equations 10 through 14 need more data: the values for K1 and K2 must be entered manually before the equation can be solved.

Current ROI means the ROI in which the cursor is located. If the cursor is Indexed to another ROI, the equation will be recalculated for that ROI.

If the spectrum is calibrated, the Peak Centroid (#5) and the FWHM (#6) will be expressed in the calibration units instead of channels. The Peak Centroid and FWHM are always included in any ROI+ASCII or ROI BRIEF hard-copy readout.

#5 Peak Centroid - Searches the current ROI for the channel number with the highest data point above the background.

#6 FWHM - Calculates the nearest whole number of channels between the left and right half-maximum points of the current ROI's peak.

#7 Counts per second - Calculates CPS for all of the displayed spectrum or for the current ROI if one has been entered.

#8 Percent error - Calculates the % error of the Area of the displayed spectrum or of the current ROI if one has been entered.

#9 Percend dead time - Calculates the spectrum's dead time to several decimal places.

#10 Half life for #11 and #13 - K1 = Half life of the isotope being measured.

#11 Efficiency - Calculates the detector's efficiency at the energy of the current ROI. Enter:

K1 = Gammas/sec for energy being measured.
K2 = Decay time in the same time units as the half life in equation 10.

#12 Activity - Calculates the current ROI's activity in microcuries. Equations #10 and #11 must be completed first. Enter:

K1 = Gammas per disintegration.

#13 Decay Corrected Activity - Corrects equation 12 for decay. Equations #10, # 11, and 12 must be completed first. Enter:

K1 = Decay time of the isotope in the same time units as the half life in equation 10.

#14 Dose rate - Calculates the dose rate in milliroentgens per hour for the current ROI. The spectrum must be Energy Calibrated in keV. Equations #10, #11, and #12 must be completed first. Enter:

K1 = Yield (gamma quanta per disintegration).
K2 = Detector to source distance in meters.

7.2 MODEL 4242 LEARN/EXECUTE

The Learn/Execute option offers a means of defining and executing a task: a sequence of Analyzer functions.

1. Up to four tasks can be learned.
2. Any one task can be executed at a time.
3. While the task is in progress, no analysis or control functions are available to the operator. Display functions can still be enabled, however.
4. Any task in progress can be terminated manually.
5. A task may be entered manually (LEARN) or by way of a previously learned task which has been stored externally (LOAD).
6. A Define/Use equation may be entered as a step by pressing USE during task entry.
7. The data collection mode (PHA or MCS) cannot be learned. The mode must be set by the operator before Execute is enabled.

7.2.1 Learn

A task is Learned (entered manually) by pressing the pushbutton associated with the desired function and completing the dialogue associated with that function. During the Learning process, the following rules apply:

A. Each task may occupy up to 64 bytes of memory. See Table 7.1.
B. The number of bytes remaining for the task will be displayed at the right side of the dialogue portion of the display (TO GO =).
C. After a step has been entered, a response of YES will move the task on to the next step.
D. The learning process will terminate if the operator presses LEARN again, disabling the function and erasing the steps so far entered.
E. If the dialogue asks if the current memory segment, as selected by the MEMORY switch, is acceptable; the only response that can be made is YES. To change to another segment, the function must be turned off, the MEMORY switch changed to another position and the function turned on again.
F. If LOAD (from an external device) is selected instead of LEARN, the operator may select TTY (Teletype) or CASsette as the device to Load from. A response of YES starts the Loading readin.
G. When the operator has completed the task entry, the dialogue allows the operator to store the task on a peripheral recording device (TTY or CAS).
H. Storing a task externally is accomplished by reading out a binary-encoded record to a Cassette tape or to a punched paper tape (TTY).
I. If, in entering a task, all of the 64 available bytes of memory are used, an attempt to enter another step will cause the message NO ROOM to be displayed. Pressing CLR will remove the message from the display and allow the operator to exit the task dialogue with a YES.

Table 7.1
BYTES PER FUNCTION

Function	Dialogue Mnemonic	Bytes Used
ENTER ROI[1]	ENTROI	6
CLEAR ROI	CLRROI	2
TRANSFER	TRANSFER	3
COLLECT	COLLECT	2
CLEAR DATA	CLRDATA	2
CLEAR TIME	CLRTIME	2
READ IN	READIN	4
READ OUT	READOUT	5
STRIP	STRIP	5
PRESET PHA	PSET PHA	11
PRESET MCS	PSET MCS	5
USE EQUATION #n[2]	USE EQU #n	2

Note[1]: in The ENTER ROI dialogue, a channel number may be entered or STORE may be pressed to enter the current cursor location.

Note[2]: an equation must be defined before entering it as a task step.

The steps are displayed only as each one is learned; the operator may want to make a list of the steps before entering them into a task to ensure that the correct steps are entered in the proper order.

At the beginning of the task and again as each step is entered, the display shows GO TO 1. This command is included in every task as the final step so that the task can be repeated from a given point (in the default case, from step one) in multiple runs of the task. Note that GO TO uses 2 of the 64 bytes.

Entering a task manually (LEARN) is simply a process of responding to the dialogue presented by the analyzer for each function as it is entered. For example:

Entering a task manually (LEARN) is simply a process of responding to the dialogue presented by the analyzer for each function as it is entered. For example:

1. Press LEARN to bring up the initial dialogue:

```
*TASK # 1
X=
                    OK?
```

The task number may be altered to 2, 3, 4 at this point.

2. Pressing YES in answer to OK? will yield the following:

```
*LEARN  # LOAD
              OK?
```

The operator must choose to enter a task manually (LEARN) or by way of a previously recorded task (LOAD).

3. A YES answer to LOAD will allow the choice of I/O device to read the task in from:

```
DEV =TTY  *CAS
              OK?
```

4. A YES answer to LEARN yields:

```
STEP  #
              OK?  TO GO = 62
```

5. To enter a function as step number one, press the pushbutton associated with the desired function. For instance, CLEAR DATA, which will start the task with a cleared memory. The display will ask if the currently selected memory segment is acceptable for the operation:

```
FULL
              OK?
```

6. Press YES to accept this step. The display will revert to:

```
STEP  2     *GO TO 1
X=
              OK?  TO GO = 60
```

7. After entering all desired functions into the task, up to the limit of 64 bytes of memory per task, the operator will answer YES to OK? to exit the task dialogue.

7.2.2 Save the Task

After the task has been defined, it may be recorded externally to be read is and used at another time. Answering YES will change the dialogue to:

```
SAVE TASK #  1
              OK?
```

A response of YES gives the operator the choice of recording device:

```
DEV=  TTY  *CAS
              OK?
```

Pressing YES allows the binary-encoded readout to start. Pressing NO bypasses the SAVE operation, leaves the task in memory, and returns the display to normal.

7.2.3 Editing The Task

After the task has been entered and accepted, it can be corrected by deleting incorrect steps or by adding omitted steps. To start the Editing process, press LEARN to see:

```
*TASK  #  1
X =
              OK?
```

The operator can change the task number through the X Register or can accept the displayed number. Pressing YES will show:

```
*LEARN     LOAD
              OK?
```

Accepting the Learn mode will show a new dialogue line:

```
USE OLD
              OK?
```

Answering NO will delete the task in its entirity; answering YES will allow the operator to review the task step by step, correcting as necessary:

1. Using the plus key (+) will advance the sequence one step at a time.
2. Using the minus key (-) will back up the sequence one step at a time.
3. Using the NO key will delete the currently displayed step.
4. Another step may be entered in the usual manner as set forth under LEARN.
5. Instead of entering a new step, + or - may be pressed to go on with the editing process.
6. During the editing process, the task will show the total number of bytes left in the task (TO GO=). This number will change only if a step in the task is changed to one using a different number of bytes or if a step is added or removed.
7. If enough bytes remain, new steps may be entered at any point in the current sequence.
8. When editing is complete, answering YES to the OK? will display the SAVE TASK dialogue as in step 7 of Section 7.2.1.

7.2.4 Execute

To begin the sequence, the operator presses EXECUTE and responds to two questions:

```
*TASK  #  1
X =
              OK?
```

The task number can be accepted or changed through the X Register. YES brings up:

```
*CYCLES = 1
X=
              OK?
```

The X Register here allows the operator to change the number of cycles of task repetition from one to any desired number between two and 255. If indefinite repetition is desired, enter 0. The task will recycle until aborted. (See Section 7.2.4)

A response of YES starts the execution of the task.

Note that the Execute function cannot be enabled while the analyzer is in Collect, Readin or Readout.

7.2.5 Stopping The Task

To stop an active Task, press EXECUTE. The dialogue will show:

*ABORT STOP CYCLES = nn
OK?

Answering YES to ABORT will stop the Task immediately. Answering YES to STOP will stop the Task at the end of the current cycle.

Note that the number of cycles remaining to be run is also displayed. If you want only to check the number of cycles remaining, press EXECute once more. This response will allow the Task to continue. Be careful not to press YES at this point or the Task will be aborted.

Section 8. Wiring Options

8.1 MODEL 4231A MIXER/ROUTER WIRING

This option allows the use of a four-input Mixer/Router (Canberra Model 8222A, or 8222B, or equivalent) with the Series 40. A single Mixer/Router expands the single-input ADC to a four-input capability. Two or four Model 8222As may be connected for up to 8- or 16-input capability.

The Mixer/Router, Model 4221 ADC and Model 4231A M/R Wiring combine to give a one, two or four input PHA and standard data acquisition capability to the Series 40. Note: The Model 4222 High Performance MCS is single input only.

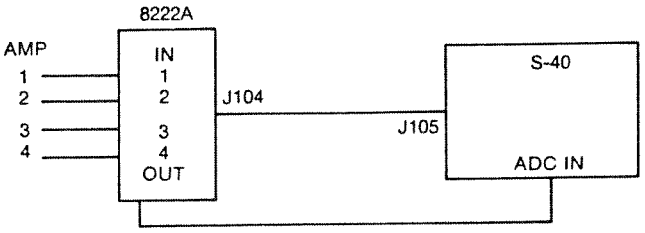
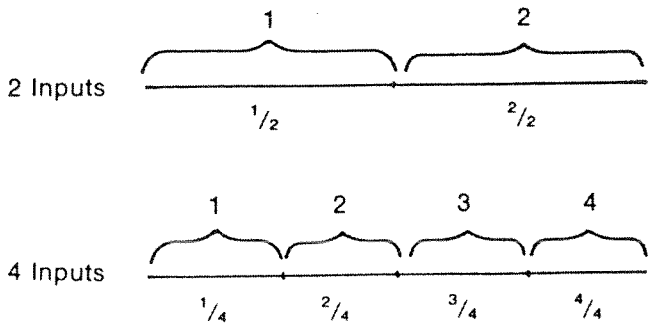
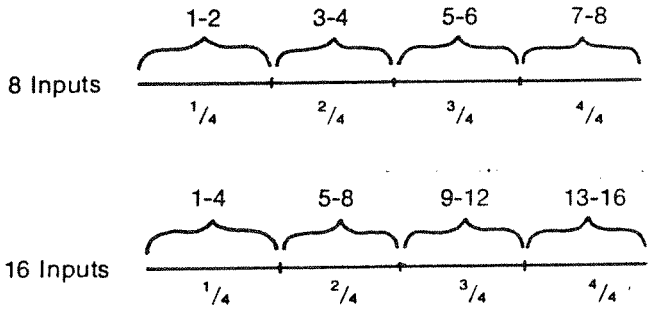


Figure 8-1 System Interconnection

The M/R button on the Series 40 enables the MCA for routing. Pressing the button allows the operator to choose how many inputs are to be routed. With the M/R function enabled, the full memory is divided into the selected number of groups. The Input Select switch on the Model 8222A Mixer/Router must set to the same number of inputs. Starting Collect will cause storage to take place:





NOTE: With early versions of the Series 40 Firmware it is possible to select 1 input. This will cause the storage in full memory regardless of the Memory control's position. With Version 2.2 and later, 1 input cannot be selected.

If only one input is to be used the Mixer/Router should not be connected because its Dead Time and Inhibit signals can affect storage.

8.2 MODEL 4232 EXTERNAL CONTROL WIRING

This option provides for Remote Control of the Series 40. TTL compatible signals on a rear panel 25-pin connector allow Mode and MCS Control and provide a Sample Changer interface.

8.2.1 Signal Description

J111 (BNC)—COUNT INput for the Model 4222 High Performance MCS.

Logic 0 < + 0.3 V at 0 mA
Logic 1 > + 3.0 V at < 1 mA
Pulse Width = 25 ns minimum
Pulse Pair Resolution = 50 ns minimum

J112 (25-pin Female D-style mating connector furnished)—Signals on this connector are all TTL compatible.

All inputs:
High + 2.4 to 5.0 V or open
Low 0.0 to +0.3 V at < 2 mA
Pulse Widths > 0.5 μs, except as noted.

All outputs:
High + 2.4 to 5.0 V at < 0.4 mA (2.4 V)
Low 0.0 to 0.5 V at < 0.4 mA.

The signals on this connector can be divided into three categories:

1. External MCS—which function with either the standard or the High Performance (Model 4222) MCS.

2. Sample Changer—which allow interfacing between the Series 40 and a Sample Changer mechanism.

3. Remote Control—which allow external control of the Series 40 when the Serial Computer Interface (Model 4273) is not required.

Note that the signal receivers and drivers are not designed for rejecting >1 V of common mode or normal mode noise. If the interconnecting cable between the Series 40 and the remote control device is greater than 3m (10 feet) in length, it may be necessary to use noise rejection to assure reliable operation. Some noise rejection techniques that have been used successfully are:

RC filtering
Twisted Pair or Coaxial Cable
Terminating resistors
Level Shifting drivers and complementary receivers
Differential drivers and receivers
Opto-isolators

8.2.2 Signal List

Connector Pin (J112)	Board Edge Connector	Signal
1		Ground
2		Ground
3		Ground
4	PC2 A-30	External Advance In
5	PC2 A-15	External Trigger In
6	PC2 A-17	Sample Changer Advance Out
7	PC4 40	MCA Busy Out
8	PC4 41	Device Busy In
9	PC4 42	Collect Out
10	PC4 44	Readout Out
11	PC4 45	Stop Collect In
12	PC4 46	Start Collect In
13	PC4 48	Clear Data In
15	PC1 29	Gate In
21	PC1 46	Abort MCS In (AMS)
22	PC1 51	Address Overflow Out (AOF)
23		Ground
24		Ground
25	PC4 52	Start Readout In

External MCS Signals

4 Ext Adv In—Logic 1 = High, Logic 0 = Low. With the MCS set for External Dwell time, the leading edge (↑) of the pulse advances the MCS address logic. In the Expand display mode, the minimum dwell is approximately 10 μs. In other modes, the minimum dwell time is 30 μs.

5 Ext Trig In—Logic 1 = High or ... Logic 0 = Low. Minimum pulse width = 1 μs. Each MCS sweep will start when the External Trigger is at Logic 1.

22 AOF Out—Logic 1 = High, Logic 0 = Low. Pulse width = 12 μs to 18 μs. Generated at the end of each MCS sweep. The next sweep will start at the end of the pulse if the External Trigger is at Logic 1.

21 AMS In—Logic 1 = High at 1 mA, Logic 0 = Low or open. Causes the MCS sweep to end and AOF to be generated. The sweep counter (channel zero) will be incremented.

15 Gate In—Logic 1 = High or open, Logic 0 = Low. Can be used to enable the Gate function of the Series 40. The function is determined by the ANTI/COINC jumper on the ADC board.

Sample Changer Interface Signals:

8 Device Busy In—Logic 1 = Low, Logic 0 = High or open. Collect can start only when this signal is at Logic 0, indicating that the Sample Changer is not busy. Collect will start about 30 ms after the signal goes to Logic 0.

6 Sample Changer Advance Out—Logic 1 = High, Logic 0 = Low. Pulse width = 75 ms to 125 ms. The Pulse is generated at the end of Collect, signalling that the Sample can be changed. The Device Busy In signal can be used to delay the start of the next Collect cycle.

External Control Signals:

7 Series 40 Busy Out—Logic 1 = Low, Logic 0 = High. Indicates that the Series 40 is not able to accept an input command. Busy goes to Logic 0 during Readout and Clear Data.

9 Collect Status Out—Logic 1 = Low, Logic 0 = High. Indicates that the Series 40 is in the Collect mode.

10 Readout Status Out—Logic 1 = Low, Logic 0 = High. Indicates that the Series 40 is in the Readout mode.

11 Stop Collect In—Logic 1 = Low, Logic 0 = High or open. Maximum pulse width = 70 μs. If the pulse is received while the Series 40 is in Collect and not Busy, Collect will end on the next increment of Live time or at the end of the current MCS sweep. Functions with the Series 40 under Computer control (REMote).

12 Start Collect In—Logic 1 = Low, Logic 0 = High or open. Maximum pulse width = 70 μs. Input to start Collect within about 30 ms using current Preset and Function (PHA or MCS) in the memory group selected by the Memory Switch. Will not be recognized or remembered if the Series 40 is Busy or under Computer control (REMote). With Version 2.2 or earlier firmware: if in Collect, this pulse will cause Collect to end. With any firmware version, the Stop Collect signal is normally used to end Collect.

13 Clear Data In—Logic 1 = Low, Logic 0 = High or open. Maximum pulse width = 70 μs. Input to clear data in the memory group selected by the Memory Switch. Will not be recognized or remembered if the Series 40 is Busy or under Computer control (REMote). Causes Series 40 Busy signal to go Low for about 200 ms.

25 Start Readout In—Logic 1 = Low, Logic 0 = High or open. Maximum pulse width = 70 μs. Input to start Readout with the current Readout parameters from the memory group selected by the Memory Switch. Will not be recognized or remembered if the Series 40 is Busy or under Computer control (REMote).

8.3 MODEL 4233 DIGITAL STABILIZER WIRING

The Model 4233 wiring option allows the Model 8200 Digital Stabilizer to be used with the Series 40's internal ADC to stabilize the ADC Gain, the ADC Zero or, with two Model 8200s, both Gain and Zero.

8.3.1 Model 8200 Modification

The Model 8200 Digital Stabilizer was designed to operate with standalone ADCs, which have address latches. With the Series 40, the ADC transfer cycle is somewhat faster than these ADCs. On older Model 8200s, therefore, the timing capacitors on the Control Logic board (PC 1) should be changed. See Appendix B.6.

On a Model 8200 shipped with the Series 40, the timing capacitors will have been changed at the factory.

8.3.2 Operation

The operation of the Analyzer and the Stabilizer and the Stabilizer is detailed in the Operator's Manual for the Model 8200. Note that:

1. The Series 40 does not provide a Live Display mode to allow window intensification. Use the cursor to determine the channel number of the reference peak's centroid. The summation of the Peak Select switches should be set to this channel number.

2. Set the Sense Switch (S20) on the Stabilizer's rear panel to "+".

3. The Ext Trigger switch on the Stabilizer must be in the OFF position. It will not be possible to inhibit storage of a reference signal.

4. Maximum correction is $> \pm 2\%$ of the Gain/Zero. It is determined by resistors on the Series 40's ADC Board. Reducing the values of these resistors will increase the correction range. Consult the factory for details.

8.3.3 Signal List

J106 Stabilizer 25-pin female D-type chassis connector.

J106 pin	ADC (PC1) pin	Signal	Description
1	24	$\overline{SA2^0}$	Latched Output from ADC Address Register Logic 1 0 V, Logic 0 = - 3 V
2	22	$\overline{SA2^1}$	
3	20	$\overline{SA2^2}$	
4	14	$\overline{SA2^3}$	
5	17	$\overline{SA2^4}$	
6	19	$\overline{SA2^5}$	
7	16	$\overline{SA2^6}$	
8	18	$\overline{SA2^7}$	
9	23	$\overline{SA2^8}$	
10	15	$\overline{SA2^9}$	
11	21	$\overline{SA2^{10}}$	
12	13	$\overline{SA2^{11}}$	
13	25	$\overline{SA2^{12}}$	
16	77	$\overline{IA1}$	Inhibit Add One Input. Logic 1 = 0 V, Logic 0 = - 3 V
20	26	STAB GAIN IN	± 5 volts, maximum
21	30	STAB ZERO IN	± 5 volts maximum
23	32	$\overline{STAB\ TRIG\ OUT}$	Logic 1 0 V, Logic 0 - 3 V
24		Ground	

8.3.4 Stabilizer Timing

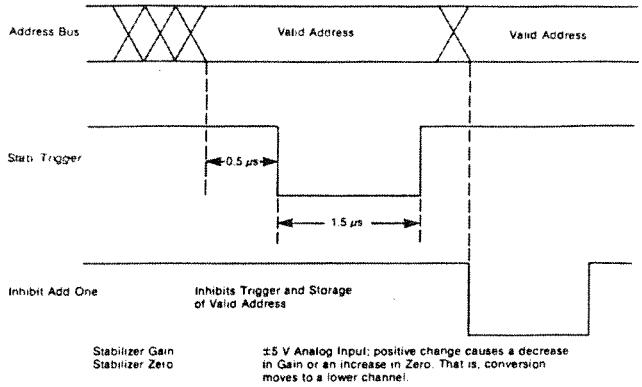

Address Bus
Valid Address
Valid Address
Stab Trigger
0.5 µs
1.5 µs
Inhibit Add One
Inhibits Trigger and Storage of Valid Address
Stabilizer Gain
Stabilizer Zero
±5 V Analog Input; positive change causes a decrease in Gain or an increase in Zero. That is, conversion moves to a lower channel.

Figure 8-3
Stabilizer Timing Diagram

8.4 MODEL 4234 PILE-UP REJECTION/ LIVE TIME CORRECTION WIRING

This optional wiring adapts the Series 40 ADC for use with a PUR/LTC Amplifier such as the Models 2013 or 2020, or equivalent. A 150 cm (five ft.) cable is provided for interconnecting the three-pin Molex-type connectors.

8.4.1 Operation With AMP/PUR/LTC

Refer to the Amplifier Manual (Model 2013, 2020 or equivalent).

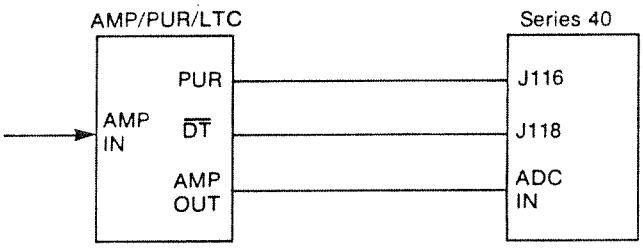


Figure 8-4
System Interconnection

The REJ jumper plug in the Amplifier should be set for a POSITIVE polarity.

The Amp/PUR/LTC module inspects the input for pile-up and permits the ADC to convert only single event signals. Signal REJ from the PUR causes the ADC to discard the pulse currently being acquired. The ADC signals this acquisition (linear gate time) to the module by output L.G. The end of LG (_┌‾) signifies that the pulse gate is now closed and the pile-up inspection circuits can be disabled. If a pulse gate has been rejected the LTC provides a busy signal (DT) to the live timer in the MCA. Refer to the Amplifier manual for details of [illegible] signal adjustments.

To illustrate the function of the Pile-Up Rejector, collect equal Live Time spectra from an active source (50 kcps) in the first half of the memory (1/2) with the PUR enabled and in the second half (2/2) with the PUR disabled. Use OVERLAP to compare the spectra. The PUR should make a significant reduction in the sum peaks and background. The resolution of the sum peaks should also be improved.

The Live Time Corrector can be illustrated by collecting a spectrum with a low rate source (A) with PUR/LTC disabled. Next add another isotope (B) with a significantly higher count rate. Collect a spectrum from the composite source for the same Live Time. Compare the photopeak of Source A in the two spectra. The AREA of this peak should be noted. Repeat the experiment with the PUR/LTC enabled. Since the activity and geometry of Source A is not changed, its peak AREA should be constant. The spectrum with the PUR/LTC enabled should show significantly less variation. Performance is dependent on factors such as spectrum energy distribution and detector geometry, size, etc. Note, the detector must be allowed to stabilize after changing the source.

8.4.2 Wiring List

Signal	Rear Panel	Wire Color	Mother Board Pin	PC
LG	J116-1	Green	G	1A-33
REJ	J116-2	Yellow	E	1A-92
Ground	J116-3	Black	A	—
BUSY (DT)	J118-1	Red	W	1A-75
Ground	J118-2	Black	Z	—

Section 9.
Signal Processing Options

9.1 MODEL 4221 AMPLIFIER/ADC

The Model 4221 is the standard Signal Processing option supplied with the Series 40. It can be supplemented by the Model 4222 High-Performance MCS option or replaced by the Model 4223 Multi-ADC Interface option. Its use is covered in sections 2, 3, and 4 of this manual.

9.2 MODEL 4222 HIGH-PERFORMANCE MCS

The Model 4222 High-Performance MCS option is used to allow a higher count rate in MCS operation. The standard MCS is limited to a count rate of about 20 kHz, maximum, while the Model 4222 allows an input count rate of up to 20 MHz.

To operate the Model 4222, the Analyzer must also contain the Model 4232 External Control Wiring option. Refer to sections 4.9 and 4.10 for MCS operating instructions and to section 5.5.2 for MCS Preset instructions.

For this option, the input signal is connected to the COUNT IN connector, which is part of the Model 4232 External Control connector, located on the rear panel. Signals and signal parameters for the Model 4232 are listed in section 8.2.

Note that if the selected dwell time is equal to or less than 30 μsec, the data portion of the display will be blanked during High-Performnance MCS Collect. This is done to allow the option more access time to the memory. The data collected will be visible on the screen when Collect ends.

9.3 MODEL 4223 MULTI-ADC INTERFACE

The Model 4223 Multi-ADC Interface allows up to four external ADCs to store PHA data in the Series 40's memory. Each ADC is provided with Preset, start/stop Collect, Clear Data and Energy Calibrate functions. Independant Live and True Timers are provided for each ADC.

A single-input Multichannel Scaling function can be performed if the Model 4222 High Performance MCS option and the Model 4232 External Control Wiring option are installed in the Analyzer.

9.3.1 SETUP

For ADC operating instructions, refer to the Operator's Manual for the ADCs being used. To connect the ADCs to the Series 40, use the 25-pin cable supplied with each of Canberra's ADCs. A 25-pin cable can be made in the field by referring to the Signal List in Section 9.3.6.

On the Series 40's rear panel, connect:
ADC # 1 to J106
ADC # 2 to J113
ADC # 3 to J114
ADC # 4 to J115

9.3.2 PHA OPERATION

The Model 4223 is capable of routing one, two or four external ADCs to the Series 40's memory. To use more than one ADC, press the M/R button on the Series 40's front panel to reveal the following dialogue:

NO. OF INPUTS *2 4
OK?

Press YES to accept two inputs or move the * by pressing NO to select four inputs.

If a single external ADC is to be routed to the memory, do not enable M/R. This will allow ADC # 1 to use the entire Series 40 memory and store in the section determined by the position of the MEMORY switch when Collect is enabled.

If two inputs have been selected, ADC # 1 will be stored in the first half of the memory and ADC # 2 will be stored in the second half.

If four inputs have been selected, each ADC will be stored in one quarter of the memory, with ADC # 1 in the first quarter, ADC # 2 in the second quarter, and so forth.

The MEMORY switch allows control of the individual inputs. With the MEMORY switch in the 1/1 position, all ADCs will be started or stopped together.

If the MEMORY switch is in the 1/2 or 2/2 position, all ADCs assigned to that half of the memory will be started or stopped together. For instance, if two inputs are selected, either of the two ADCs may be started or stopped independantly. If four inputs are selected, ADCs 1 and 2 or 3 and 4 may be started or stopped together. With the MEMORY switch in the 1/4, 2/4, 3/4, or 4/4 position, each of the four ADCs may be started or stopped independantly.

Note that if the MEMORY switch is set to an inactive region of the memory, the display will show the Canberra logo. If the MEMORY switch is set to an active section of memory, the Dead Time Meter will be displayed, showing that the region is collecting.

In a similar manner, the MEMORY switch position will control the use of a region's Preset, Clear Data/Clear Time or Energy Calibrate functions.

The Series 40's Firmware checks the ADCs at about a one microsecond scan rate to see if any ADC's conversion is complete. The first ADC found ready will have its converted address gate onto an address bus. If the address is within the ADC's assigned range, is not inhibited by $\overline{\text{INHAD}}$ (see the Signal List) and is not channel address zero or one, a PHA ±1 cycle is performed. The Data Accepted signal is then generated to release the ADC for another conversion. Note that the address from the ADC must be stable during the entire memory cycle.

The ADC is prevented from storing an address beyond its assigned memory group. In order to minimize ADC dead time, the ADC's RANGE switch should be set to equal the assigned memory size for that ADC.

9.3.3 MCS OPERATION

Single-input MCS operates as described in the Multichannel Scaling operating instructions (Sections 4.9 and 4.10). To perform single-input MCS data acquisition, the M/R function on the front panel must be turned off.

A jumper plug on the Model 4223 Interface Board is provided for inverting the Count Enable Gate polarity. In the COINCidence position, an open connector (nothing connected) or a positive TTL level will enable counting; a TTL low level or ground will disable counting.

In the ANTIcoincidence position, an open connector or a positive TTL level will disable counting; a TTL low level or ground will enable counting.

9.3.4 MIXER/ROUTER OPERATION

The Model 8220 or 8222 Mixer/Router can be used with any of the external ADCs to provide routing of up to 16 inputs to the memory. Using the Mixer/Router will allow its inputs to be routed to that ADCs memory segment. See the Mixer/Router Operator's Manual for complete instructions.

9.3.5 BOARD JUMPERS

See Figure 9-2.

ANIT-COINC - Discussed in section 9.3.3, MCS Operation.

A-B - Used for testing only. Leave in the B position.
MUX-EXT ADC - Not currently used. Leave in the MUX position.

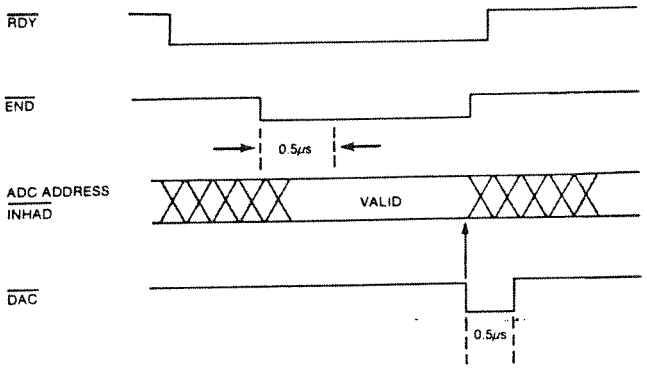


Figure 9-1
PHA Cycle Timing Diagram

9.3.6 SIGNAL LIST

Chassis connectors (J106, J113, J114, J115): female 25-pin; Amphenol type 17-10250.

Logic levels:
Logic HI = +2.4 to +5 volts;
Logic LO = 0.0 to +0.3 volts.

Pin	Signal	Description
1	$\overline{2^0}$	ADC Address input; Logic 1 = LO; 2^0 to 2^{11} require positive drive 2^{12} has a pull-up resistor on its input for use with 12 bit ADCs.
2	$\overline{2^1}$	
3	$\overline{2^2}$	
4	$\overline{2^3}$	
5	$\overline{2^4}$	
6	$\overline{2^5}$	
7	$\overline{2^6}$	
8	$\overline{2^7}$	
9	$\overline{2^8}$	
10	$\overline{2^9}$	
11	$\overline{2^{10}}$	
12	$\overline{2^{11}}$	
13	$\overline{2^{12}}$	
14	$\overline{\text{RDY}}$	ADC Conversion Ready input; Logic 1 = LO; open circuit = Logic 0.
16	$\overline{\text{INHAD}}$	Inhibit Storage of Current Conversion input; Logic 1 = LO, open circuit = Logic 0.
17	$\overline{\text{DAC}}$	Data Accepted output; 0.5 μsec pulse; Logic 1 = LO.
21	DT	ADC Dead Time input; Logic 1 = HI; open circuit = Logic 0.
22	$\overline{\text{END}}$	Enable ADC Address output; Logic 1 = LO.
24	GND	Ground

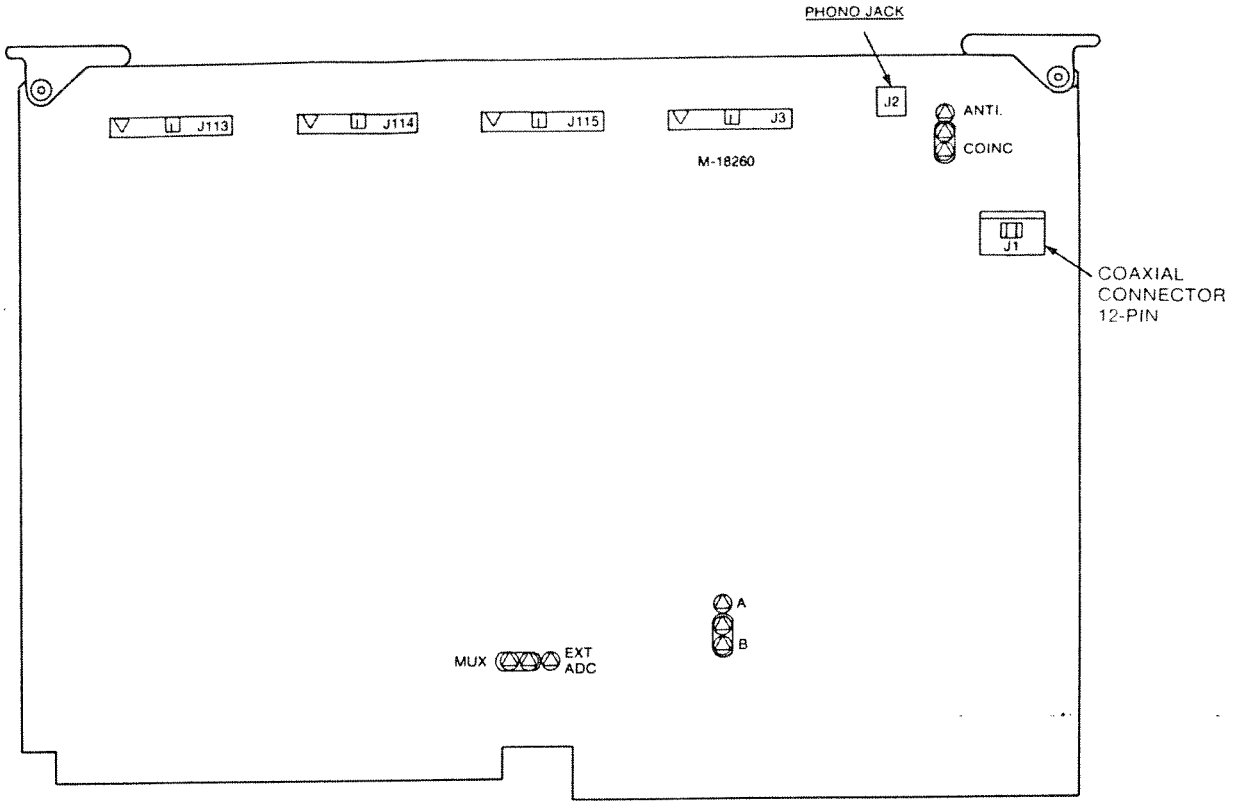


Figure 9-2
Model 4223 Interface Jumpers

Appendix A.
Internal Controls and Connector Signals

This section provides information that will be helpful in case of equipment malfunction. With common test equipment, such as an oscilloscope and a voltmeter, and reference to the information contained in this section, it will usually take no more than a telephone call or a letter to Canberra's Customer Service Department or International Representative to quickly effect repair of the equipment.

NOTE: Internal controls and jumpers that are not specifically mentioned in the following sections are for test purposes or for factory installed options. They must not be moved.

A.1 OPERATING VOLTAGE SELECTION (Figure A-1)

To change the operating voltage of the analyzer, move the plastic fuse shield, next to the ac line cord socket, to one side. The voltage selection printed circuit card (J4) is located just below the fuse. The operating voltage the analyzer is set for will be visible on the card.

To change between 120 and 240 volts or to change to low-line voltage (100 or 220 volts), pull J4 out of its socket with a pair of needle-nose pliers and replace it so that the desired voltage is visible beneath the fuse.

Be certain to check the fuse rating when changing the operating voltage; a change from 100/120 volts to 220/240 volts, or the reverse, will require a change of fuse to the proper rating as well. See Table A-1.

J4 Position	Operating Range	Line Fuse Rating
100	85 V to 110 V	2 Amp slow-blow
120	105 V to 130 V	2 Amp slow-blow
220	190 V to 240 V	1 Amp slow-blow
240	210 V to 260 V	1 Amp slow-blow

Table A-1
Series 40 Line Voltage Selection

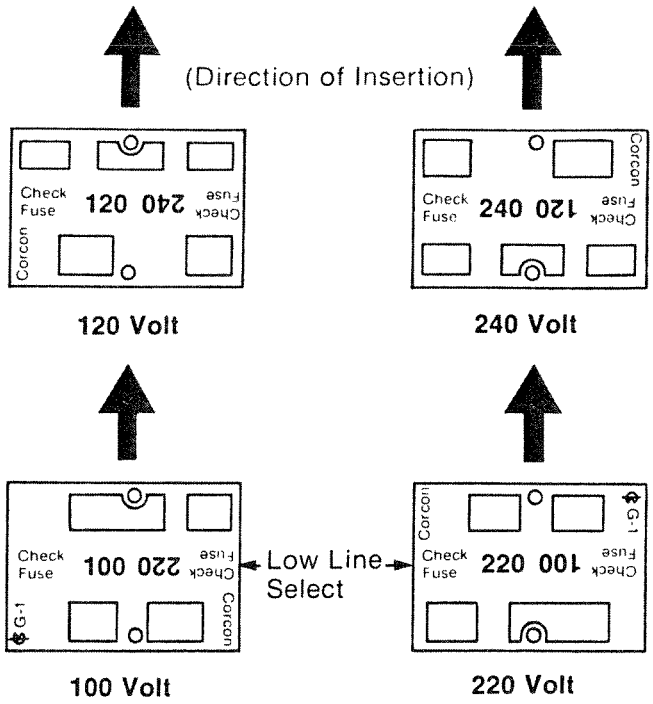


Figure A-1
J4. Line Voltage Selection Card

A.2 CPU BOARD (Figure A-2)

If the Model 8681 Standby Power Supply is to be used, the + 5 volt and + 12 volt jumpers in the lower left corner of the board must be moved to the STBY position, toward the center of the board.

The only other jumper that is of concern is the 50 Hz wire jumper located just above and to the right of the STBY jumpers. It must be in place in areas that have a line frequency of 50 Hz and must be removed if the analyzer is to be used in 60 Hz areas. It is used to define the time base for the True time clock.

A.3 ADC BOARD (Figure A-3)

AN/CO jumper to select ANticoincidence gating or COincidence gating. Shipped in the CO position.

PHA/SVA jumper to select Pulse Height Analysis or Sampled Votage Analysis mode. shipped in the PHA position.

V/C jumper (accessable through a slot in the metal cover in the upper right corner of the board) to select the Voltage sensitive input mode or the Charge sensitive input mode. Shipped in the V position.

P/N jumper to select Positive inputs or Negative inputs in the Voltage sensitive mode only. Shipped in the Positive position.

J7, (or A52) in the lower left corner of the board, receives a plug for the Model 4231 Mixer/Router option. The plug, which is shipped with the option, is configured for a particular memory size; it must be used for that memory size only.

A.4 DISPLAY BOARD AND MONITOR

The only user control on the Display board is the Test Switch, S1, located at the rear of the top edge of the board. Depressing this switch will superimpose a test pattern, composed of rows of dots, on the screen. Its primary use is in checking the linearity of the monitor.

The switch may be locked in the test position by rotating it clockwise after it has been depressed. The switch must be restored to its normal, unlocked, position before proceeding with normal operation of the analyzer.

There is a connector on the monitor's CRT. Its pinout, from right to left when connected to the CRT, is:

Pin	Signal
1	+ 15 volt return and LSYNC return
6	LSYNC
7	+ 15 volt supply
8	VIDEO
9	$\overline{\text{FSYNC}}$
10	VIDEO return and $\overline{\text{FSYNC}}$ return

A.5 MISCELLANEOUS LOGIC BOARD (Figure A-4)

C IN/C OUT jumper controls the transmission of control (CTL) characters to a peripheral device. CTL is used by the Series 40 during Readin. Some Readout-only devices will not accept CTL. The jumper is shipped in the C IN position, which enables transmission of CTL. If the peripheral device to be used with the Series 40 will not accept CTL, the jumper must be moved to the C OUT position. If a peripheral device is ordered from Canberra at the same time as the Series 40, the jumper will be positioned correctly for that device.

Jumper A-B controls signal Ready. In the A position, DTR (Data Terminal Ready) generates Ready. Position B allows either DTR or RRDY (Receiver Buffer Empty) to generate Ready; used with faster EIA devices. Shipped in the A position.

Jumper C-D controls signal Interrupt. In the C position, TXMT (Transmitter Buffer Empty) signals the USART Interrupt. In the D position TRDY (Transmitter Empty) signals the USART Interrupt; used with faster EIA devices. Shipped in the C position.

Jumper E-F controls the polarity of the BUSY flag, which is used to enable the Model 5411 Digital Cassette Recorder's tape drive motor and to provide a Busy indication to an EIA device during Readin. Shipped in the E position. If a flag of the opposite polarity (BUSY) is required, the jumper must be changed to the F position.

Jumper G-H is to be in the H position unless Model 4231 Mixer/Router Wiring is installed, in which case the jumper must be moved to the G position.

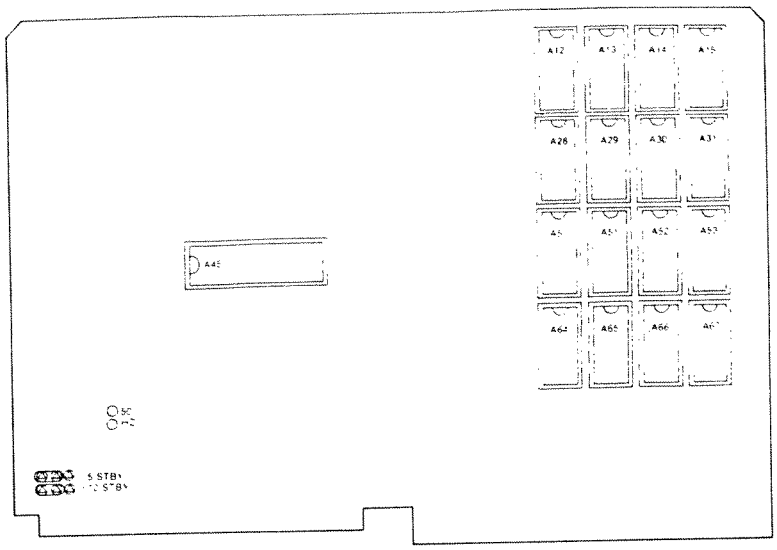


Figure A-2
CPU Board

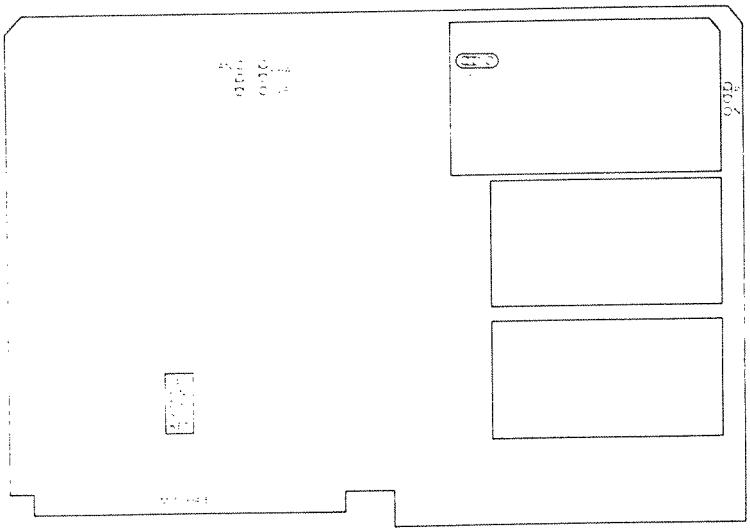


Figure A-3a
Early ADC Board

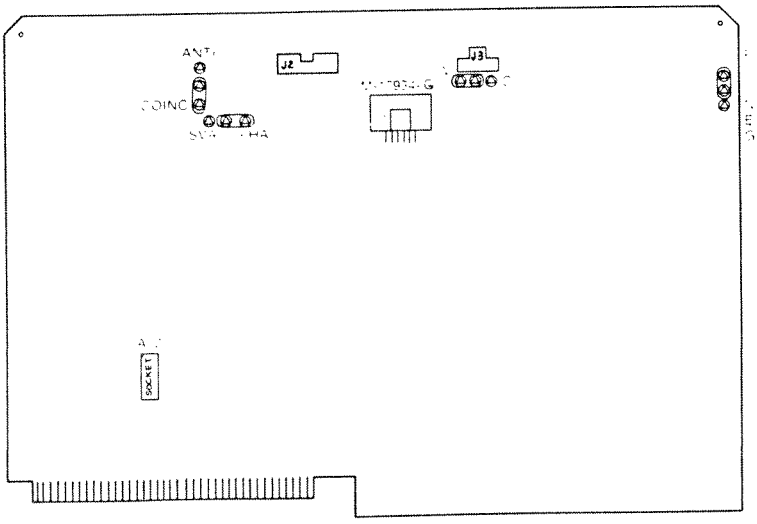


Figure A-3b
Revision G ADC Board

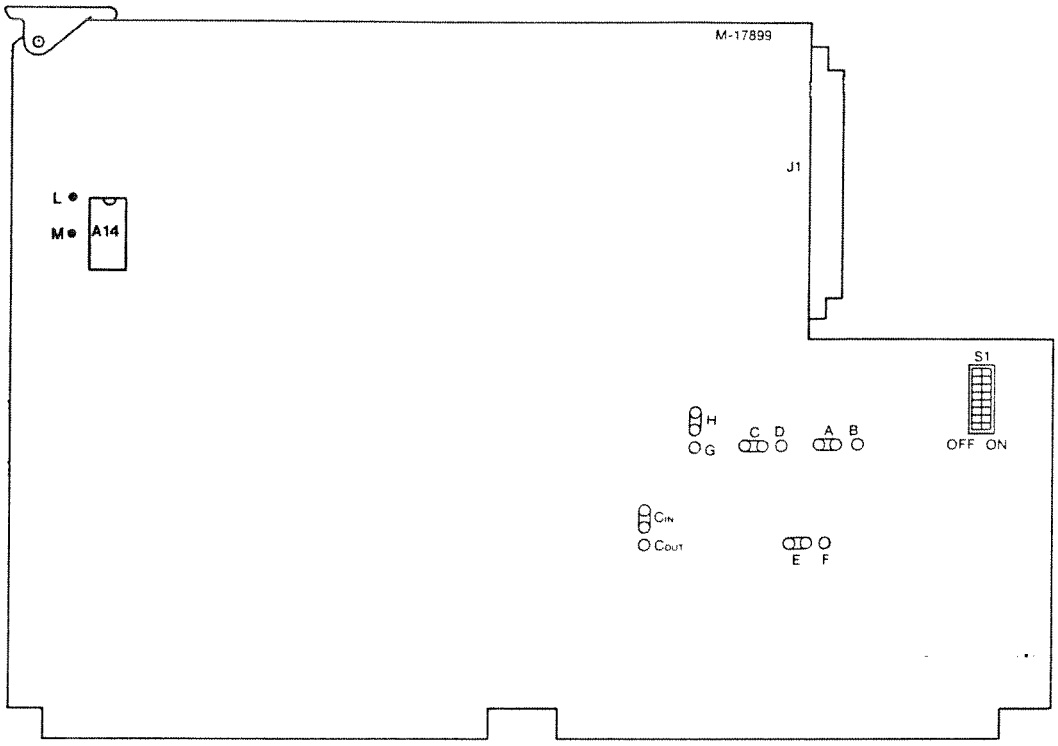


Figure A-4
Miscellaneous Logic Board

The DIPswitch, S1, controls several functions concerned with data I/O, as follows:

Shipped	Number	Function	On	Off
ALL OFF	1-3	Set EIA rate	See Table A.2	
ON	4	EIA rate	Variable rate	110 baud
ON	5	Parity select	Enable	Disable
ON	6	Parity	Even	Odd
OFF	7	TTY rate	300 baud	110 baud
ON	8	CAS/EIA	Cassette	EIA device

Baud Rate	Switch Numbers		
	1	2	3
300	OFF	OFF	OFF
600	ON	OFF	OFF
1200	OFF	ON	OFF
2400	ON	ON	OFF
4800	OFF	OFF	ON
9600	ON	OFF	ON

Table A.2
Standard I/O Baud Selection

Note: switches 7 and 8 can be set to the OFF po[illegible] and, by grounding the appropriate pins on J101, can be remotely set to the ON position. See the note at the end of the signal list for J101 in section A.9.1 - EIA Connector. With switch 8 in the OFF position, the I/O dialogue will read EIA instead of CAS.

The Model 5421's Interface can be used for both the cassette and an EIA device. When the interface's TERMINAL/CASSETTE switch is moved "out", the Analyzer will be set for cassette operation.

A.6 LOW VOLTAGE POWER SUPPLY

The Low Voltage Power Supply has five LED indicators at the top of the board which show that each supply is functioning. The indicators, from front to back, are:

+5 volts
-24 volts
+24 volts
+12 volts
-12 volts

Connector J1, also at the top of the board, has the following pinout:

Pin	Signal
1	ac to + 5 regulator
2	ac to + 5 regulator
3	ac return from + 5 regulator
4	ac return from + 5 regulator
5	ac return from < ± 12 and + 15 regulators
8	+ 24 volts to preamp connector
11	preamp connector ground
12	HVPS connector ground
13	ac to ± 24 regulator
14	ac to + 5 regulator
15	ac return from + 5 regulator
16	ac to ± 12 and + 15 regulators
17	ac to ± 12 and + 15 regulators
18	ac return from ± 12 and + 15 regulators
20	+ 24 to HVPS connector
21	-12 volts to preamp connector
22	+ 12 volts to preamp connector
23	-24 volts to preamp connector
24	ac return from ± 24 regulator
25	ac return from ± 24 regulator

A.7 X-Y PLOTTER BOARD (Figure A-5)

Control NABL is a factory set for low level true. To invert this level, change jumper B-C to B-A.

Control SEEK is factory set for high level true. To invert this level, change jumper E-F to E-D.

The pinout of the 25-pin connector at the top of the board is the same as the pinout of the X-Y Plotter connector (J107 or J108) on the analyzer's rear panel.

For line plotters that do not provide an Advance output, the plot rate can be adjusted from 2 to > 10 channels per second with RV1. Line plotters without an external disable must have their servos turned OFF when not in the Plot mode.

A.8 SERIAL INTERFACE BOARD (Figure A-6)

The 52/53/73 jumper defines the use of this board; the jumper must be in the 52 position for use with the Model 4252 Printer/Plotter Interface, in the 53 position for use with the Model 4253 Graphics Plotter Interface or in the 73 position for use with the Model 4271 or 4273 Computer Interface.

The C-D jumper must be in the position specified in the option's operating instructions.

The H-I jumper must be in the H position for the Model 4271 or 4273 Computer Interface. Other options use the I position.

The Serial Interface board is shipped with no M-N jumper installed.

For the Model 4252, the jumper enables transmission of control (CTL) characters. With the jumper out or in the N position, CTL transmission is enabled.

For readout-only devices which will not accept CTL, insert a wire jumper in the M position to inhibit CTL.

For the Model 4253, the M-N jumper controls plot mode. With the jumper out or in the N position, the line-plot mode is enabled. With the jumper in the M position, the point-plot mode is enabled.

For the Models 4271 and 4273/A/B the M-N jumper has no effect.

The DIPswitch at the bottom of the board controls several functions as defined below:

Number	Function	On	Off
1-4	Set baud rate	See table A.3	
5	Characters	7 Characters	8 Characters
6	Parity Select	Disables	Enables
7	Parity	Odd	Even
8	Stop Bits	One	Two

Table A.3
Serial I/O Baud Rate Selection

Baud Rate	Switch Numbers			
	1	2	3	4
75	OFF	ON	ON	ON
110	ON	OFF	ON	ON
134.5	OFF	OFF	ON	ON
150	ON	ON	OFF	ON
300	OFF	ON	OFF	ON
600	ON	OFF	OFF	ON
1200	OFF	OFF	OFF	ON
1800	ON	ON	ON	OFF
2000	OFF	ON	ON	OFF
2400	ON	OFF	ON	OFF
3600	OFF	OFF	ON	OFF
4800	ON	ON	OFF	OFF
7200	OFF	ON	OFF	OFF
9600	ON	OFF	OFF	OFF
19200	OFF	OFF	OFF	OFF

For the External Clock option (available by special order), set all switches to ON.

See the option's operating instructions for the correct switch settings.

The connector at the top of the board has the following pinout:

For RS 232 (Models 4252, 4253, 4271, and 4273A):		For RS 422 (Model 4273):	
Pin	Signal	Pin	Signal
A	Ground	LL	Clear to send +
M	Data in	KK	Clear to send -
C	Data out	PP	Carrier detect +
L	RTS	RR	Carrier detect -
H	CTS	TT	Data set ready +
D	DSR	SS	Data set ready -
B	Ground	NN	Data out +
J	DCD	MM	Data out -
K	Flag	VV	Ground
N	DTR	UU	Ground
E	Busy	CC	Data in +
Z	422 In	DD	Data in -
X	Ground	FF	Data term ready +
Y	422 Out	EE	Data term ready -
W	Ground	HH	Request to send +
		JJ	Request to send -
		AA	Ground
		BB	Ground

A.9 MAG TAPE INTERFACE BOARD

The ABC, DEF, and GHI jumpers define the data-block size. Factory set to 256 channels per block.

Block Size	Jumper Configuration		
note[1]	B-C	E-F	H-I
256	A-B	E-F	H-I
512	B-C	D-E	H-I
1024	A-B	D-E	H-I
2048	B-C	E-F	G-H
4096	A-B	E-F	G-H
8192	B-C	D-E	G-H
note[2]	A-B	D-E	G-H

Note[1]: not valid; defaults to 256.
Note[2]: not valid; defaults to 8192.

The XYZ jumper allows the interface to record a time-of-readout Tag: a six-character Time-of-Day Code followed by a six-character Data Code at the start of each block. Factory set to disable the Tag Word.

Position	Tag Word
Y-Z	Disabled
X-Y	Enabled

The KLM jumper is set to K-L to enable communication between the interface and the Model 8531A Controller. The L-M position is not currently used.

The 2716/2732 jumper is set to 2716, the type of chip in socket A50. The 2732 position is not currently used.

A.10 GPIB INTERFACE BOARD

The GPIB board has one jumper, which must always be in the B0 position, and an 8-pole rocker switch. Refer to the Model 4272 GPIB Interface manual for the switch settings. See Figure B-14.

A.11 REAR PANEL CONNECTORS. (Figure A-7)

Jack#	Function	Connector Size
J101	EIA (RS232)	25 pin
J102	TTY	9 pin
J103*	Standby Power	15 pin
J104	AC Power In	— —
J105*	Mixer/Router	25 pin
J106*	Stabilizer/Ext ADC	25 pin
J107* }	I/O Options (any 2)	25 pin
J108* }	4251, -52, -53, -54, -71, -72, -73	25 pin
J109*	HVPS Power Enable	3 pin
J110	Preamp Power	9 pin
J111*	Remote	BNC
J112*	Remote	25 pin
J113*	Multiplexed Ext ADC	25 pin
J114*	Multiplexed Ext ADC	25 pin
J115*	Multiplexed Ext ADC	25 pin
J116*	Pileup Rejector	3 pin
J118*	Pileup Rejector	BNC

*Option

Note 1: J116, and J118 are assembled on one plate; identified "PUR"

Note 2: J111 and J112 are assembled on one plate; identified "REMOTE"

Note 3: The Remote option is necessary for the Model 4222 High Performance MCS option.

Note 4: The Model 4272 connector has 24 pins.

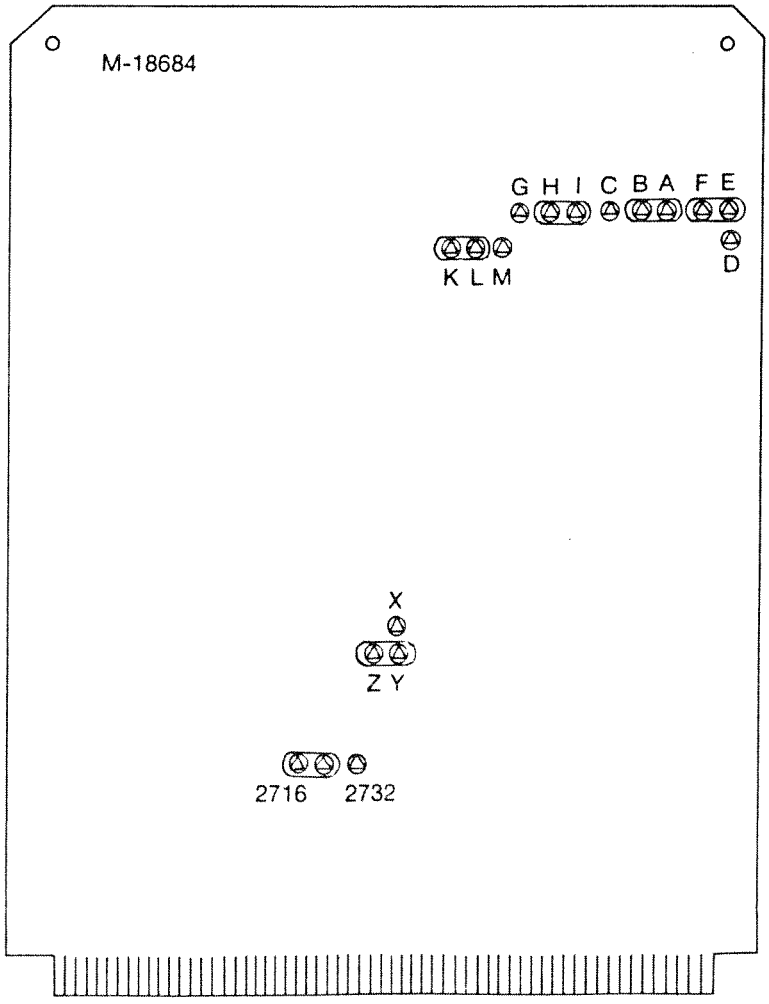


Figure A.5
Tape Interface Board

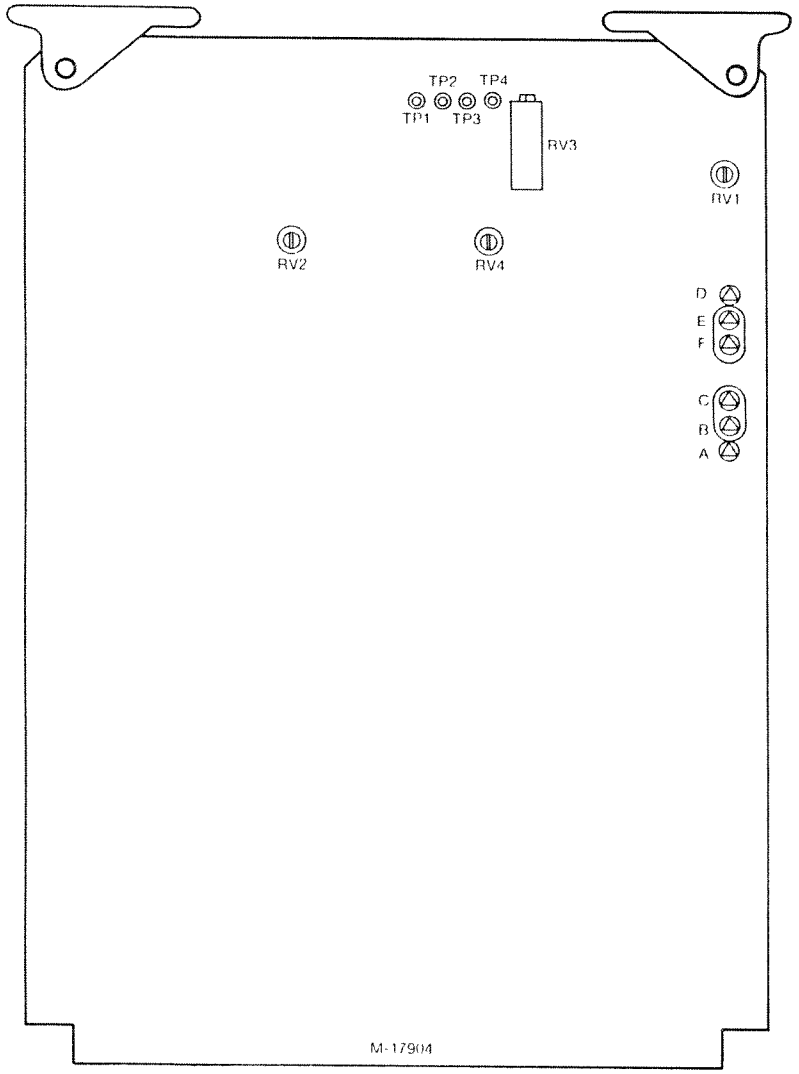


Figure A-6
Plotter Interface Board

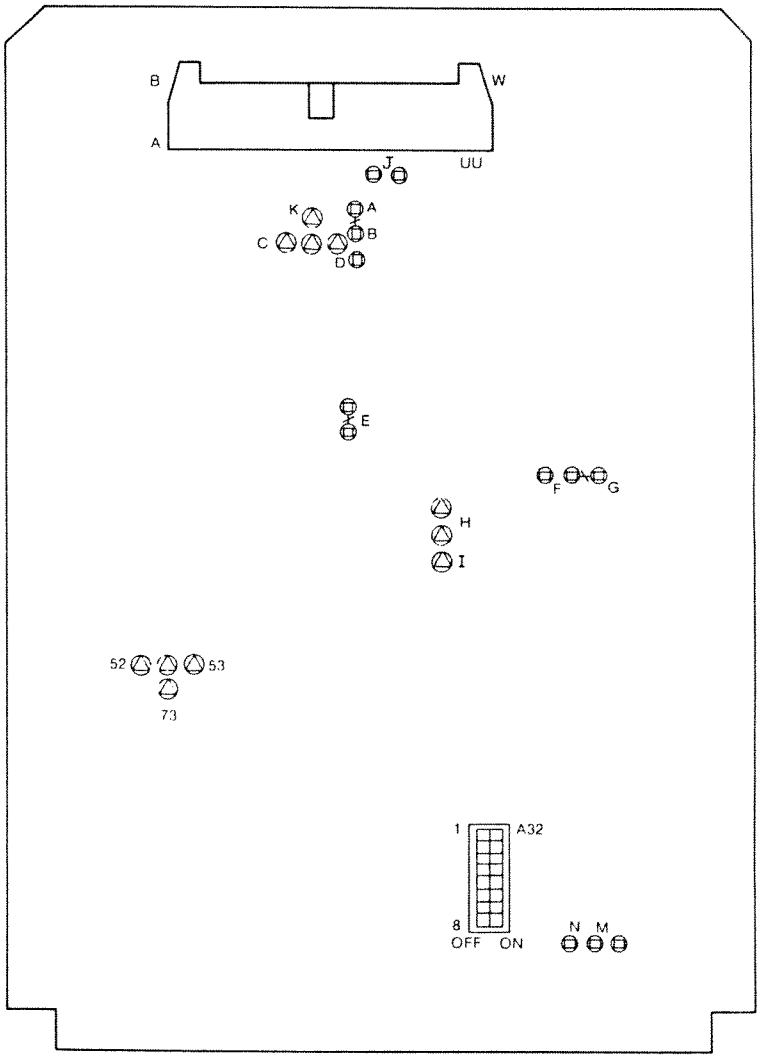
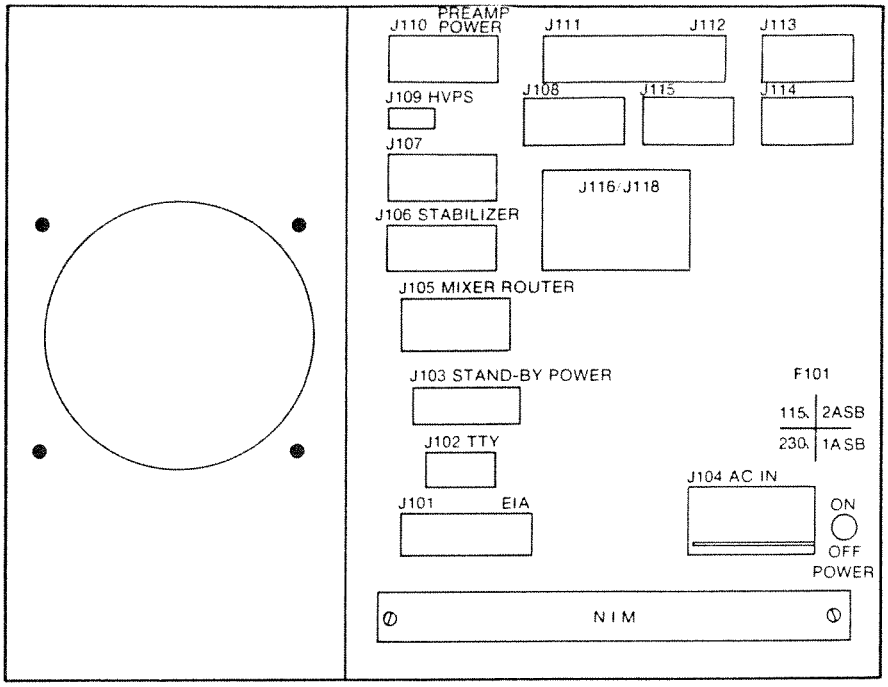


Figure A-7
Serial Interface Board



Location	Designation
J101	EIA Connector
J102	Teletype Connector
J103	Stand-by Power Supply
J104	AC Line Input
J105	Mixer Router
J106	Stabilizer Data External ADC 1
J107/J108	I/O Options
J109	High Voltage Power Supply
J110	Preamplifier Power Supply
J111/J112	Option 4222/4232
J113/J114/J115	ADC Multiplexer Inputs
J116/J118	Pile-up Rejector

Figure A-8
Series 40 Rear Panel

A.11.1 J101 - EIA Connector Signals:

Pin	Signal	Description
1	AA	Ground
2	BA	Received data (in from device)
3	BB	Transmitted data (out to device)
4	CA	Ready to send (in from device)
5	CB	Clear to send (out to device)
6	CC	Data set ready
7	AB	Ground
8	CF	Received line signal detector
11	- -	Flag (in from device)
18	- -	5411 external enable
20	CD	Data terminal ready
23	- -	TTY baud select
25	- -	Busy (to device)

Note: normally the TTY baud rate is set at 110 baud. If the user wishes to alternate between current-loop (TTY) devices that operate at 110 baud and 300 baud, switch 7 on the Miscellaneous Logic board can be set to OFF (110 baud). Externally grounding pin 23 of J101 will allow the TTY to operate at 300 baud.

In the same manner, EIA/CAS enable is normally set for CAS. Setting switch 8 to the OFF position (EIA enabled) allows J101 to be used for an EIA type device. See section A.5 for setting EIA baud rates. Externally grounding pin 18 of J101 will allow the connector to be used for the Cassette.

A.11.2 J102 Teletype Signals

Pin	Signal	Description
1	TTY Sol -	Motor Start Return
2	Tx +	Transmit
3	Gnd	Ground
4	TTY Sol +	Motor Start
6	Rx -	Receive Return
7	Rx +	Receive
9	Tx -	Transmit Return

A.11.3 J103-Standby Power Supply Signals

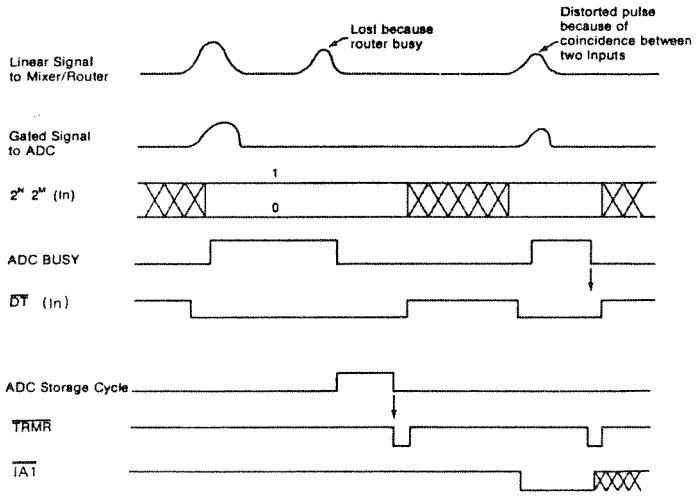
Pin	Signal	Description
1	$\overline{PRS}$	Power Reset
3	STBY 5V	Standby + 5 volts
4	STBY 12V	Standby + 12 volts
8	$\overline{PWRF}$	Power Fail
9	GND	Ground
11	24 RET	+ 24 volt return
12	+ 24V	+ 24 volt supply

A.11.4 J105 Mixer/Router Signals

Pin	Signal	Description	Direction referred to Series-35
1	$\overline{EG3}$	Enable Group 3	Out
2	$\overline{HIMR}$	High Performance M/R	In
3	$\overline{RA}$	Time Code Bit 0	
4	$\overline{MRAK}$	Time Code Transfer Complete	Out
5	RB	Time Code Bit 1	In
6	EG4	Enable Group 4	Out
7	$\overline{EG2}$	Enable Group 2	Out
8	$\overline{IND}$	Enable 16 Inputs	Out
9	$2N^{-2}$	Routing Code Bit 0	In
10	$2N^{-1}$	Routing Code Bit 1	In
11	2N	Routing Code Bit 2	In
12	2M	Routing Code Bir 3	In
13	$\overline{INA}$	Enable 2 Inputs	Out
14	$\overline{TRMR}$	ADC Conversion Complete	Out
15	$\overline{CTM}$	Clear Timers	Out
16	$\overline{IA1}$	Inhibit Add 1	In
17	$\overline{TRMR}$	ADC Conversion Complete	Out
18	$\overline{EG1}$	Enable Group 1	Out
19	$\overline{MRTT}$	Time Tick Ready	In
20	GND	Ground	—
21	$\overline{DT}$	Dead Time	In
22	GND	Ground	—
23	INB	Enable 4 Inputs	Out
24	GND	Ground	—
25	$\overline{INC}$	Enable 8 Inputs	Out

Signal Levels

High (H) =2.4 to =5 volts at <0.4mA (2.4 V)
Low (L) 0.0 to 0.3 volts at 2 mA



Timing Diagram

Address Routing

1 = > +3.0V
0 = < +0.3V
X = don't care

Inputs	Memory	2^M	2^N	2^{N-1}	2^{N-2}
1	Full	x	x	x	x
2	1/2	0	x	x	x
	2/2	1	x	x	x
4	1/4	0	0	x	x
	2/4	0	1	x	x
	3/4	1	0	x	x
	4/4	1	1	x	x
8	1/4	0	0	0	x
		0	0	1	x
	2/4	0	1	0	x
		0	1	1	x
	3/4	1	0	0	x
		1	0	1	x
	4/4	1	1	0	x
		1	1	1	x
16	1/4	0	0	0	0
		0	0	0	1
		0	0	1	0
		0	0	1	1
	2/4	0	1	0	0
		0	1	0	1
		0	1	1	0
		0	1	1	1
	3/4	1	0	0	0
		1	0	0	1
		1	0	1	0
		1	0	1	1
	4/4	1	1	0	0
		1	1	0	1
		1	1	1	0
		1	1	1	1

A.11.5 J106 Stabilizer Data/External ADC: (operates with Model 8200)

Pin	Signal	Description
1	$SA2^0$	Gated Binary Address Data
2	$SA2^1$	
3	$SA2^2$	
4	$SA2^3$	
5	$SA2^4$	
6	$SA2^5$	
7	$SA2^6$	
8	$SA2^7$	
9	$SA2^8$	
10	$SA2^9$	
11	$SA2^{10}$	
12	$SA2^{11}$	
13	$SA2^{12}$	Gated Binary Address Data
14	ADCRDY	ADC Ready
16	IA1	Inhibit Add One
17	DACCP	Data Accept
20	STAB GAIN	Stabilizer Gain (± 5V)
21	STAB ZERO	Stablizer Zero (± 5V)
22	ENDATA	Enable Data
23	STAB TRIG	Stabilizer Trigger
24	GND	Ground

A.11.6 J107 and J108

These Connectors are used for any two of the following I/O options:

Model Number	Interface Type
4251	X-Y Point Plotter
4252	EIA Printer/Plotter
4253	Graphics Plotter
4254	Magnetic Tape
4271	Computer Interface
4272	GPIB Interface
4273	Jupiter Interface

Model 4251 Connector:

Pin	Signal	Description
2	XGND	X Ground
4	YGND	Y Ground
5	SEEK	Coordinate Control Out
6	CPC	Completed Plot Control In
9	NABL	Plotter Enable Out
14	GND	Ground
21	PLTY	Y Plot
23	PLTX	X Plot

Model 4252/4253 Connector (RS232):

Pin	Signal	Description
1	GND	Ground
2	DATA IN	Received Data from device
3	DATA OUT	Transmitted Data to device
4	RTS	Ready to Send from device
5	CTS	Clear to Send to device
6	DSR	Data Set Ready
7	GND	Ground
8	DCD	Received Line Signal Detect
11	FLAG	Flag from device
20	DTR	Data Terminal Ready
25	BUSY	Busy to device

Pin 11: a TTL or RS232 low level input to the device stops data output after the current character. A high level signals device Ready.

Model 4254 Connector

Pin	Signal	Direction referred to Series 40
1	$\overline{WD1}$	Out
2	$\overline{WD0}$	Out
3	$\overline{WD2}$	Out
4	$\overline{WD3}$	Out
5	GND	—
6	$\overline{GND}$	—
7	$\overline{RD3}$	In
8	$\overline{RD2}$	In
9	$\overline{GND}$	—
10	$\overline{RD1}$	In
11	$\overline{RD0}$	In
12	$\overline{BCD}$	Out
13	$\overline{RI}$	Out
14	$\overline{ESPI}$	Out
15	$\overline{RO}$	Out
16	$\overline{ADDRESS}$	Out
17	$\overline{MT}$	Out
18	$\overline{ADRNO}$	In
19	$\overline{I/O\ ATX}$	In
20	$\overline{GAP}$	In
21	$\overline{SP}$	In

Model 4271 Connector (RS232)

Pin	Signal	Direction, referred to Series 35
1	Ground	----
2	Data In	In
3	Data Out	Out
4	Request to Send (RTS)	In
5	Clear to Send (CTS)	Out
6	Data Set Ready (DSR)	Out
7	Ground	----
8	Carrier Detect (CD)	Out
11[1]	Flag	In

[1]Active input normally on Pin 11. Internal jumper to use pin 4.

Model 4272 GPIB Connector

Pin	Signal	Description
1	DIO1	Data I/O 1
2	DIO2	Data I/O 2
3	DIO3	Data I/O 3
4	DIO4	Data I/O 4
5	EOI	End or Identify
6	DAV	Data Valid
7	NRFD	Not Ready for Data
8	NDAC	Not Data Accepted
9	IFC	Interface Clear
10	SRQ	Service Request
11	ATN	Attention
12	Shield	To Earth Ground
13	DIO5	Data I/O 5
14	DIO6	Data I/O 6
15	DIO7	Data I/O 7
16	DIO8	Data I/O 8
17	REN	Remote Enable
18	Twisted Pair with pin 6	
19	Twisted Pair with pin 7	
20	Twisted Pair with pin 8	
21	Twisted Pair with pin 9	
22	Twisted Pair with pin 10	
23	Twisted Pair with pin 11	
24	Signal Ground	

Model 4273 Connector (RS422)

Pin	Signal	Direction referred to Series 40
1	GND	---
3	Received Data +	In
6	Request to Send +	In
8	Clear to Send-	Out
10	Data Set Ready +	Out
11	Terminal Ready +	In
12	Carrier Detect +	Out
13	GND	---
14	GND	---
15	Received Data-	In
17	Transmitted Data-	Out
18	Request to Send-	In
20	Clear to Send +	Out
22	Data Set Ready-	Out
23	Terminal Ready-	In
24	Carrier Detect-	Out
25	GND	---

Models 4273A, 4273B Connector (RS232)

Pin	Signal	Direction, referred to Series 40
1	Ground	---
2	Data In	In
3	Data Out	Out
4[1]	Request to Send (RTS)	In
5	Clear to Send (CTS)	Out
6	Data Set Ready (DSR)	Out
7	Ground	---
8	Carrier Detect (CD)	Out
11	Flag	In
20	Data Terminal Ready (DTR)	In
25[2]	Busy	Out

[1] Active input normally on pin 4. Internal jumper to use pin 11.
[2] No function in this interface.

A.11.7 J109 High Voltage Power Supply Connector

Pin	Signal	Description
1	GND	Ground
2	+ 24	+ 24 volt dc supply
3	---	No connection

A.11.8 J110-Preamp Power Connector

Pin	Signal	Description
1	GND	Ground
2	GND	Clean Ground
4	+12	+12 volt dc supply
6	-24	-24 volt dc supply
7	+24	+24 volt dc supply
9	-12	-12 volt dc supply

A.11.9 J111 and J112-Remote Connector

Pin	Signal	Description
J111-BNC	COUNT	MCS Count Input (Model 4222)
J112:		
1	GND	Ground
2	GND	Ground
3	GND	Ground
4	EXT ADV	MCS External Advance In
5	EXT TRIG	MCS External Trigger In
6	SCADV	Sample Changer Advance Out
7	BSYOUT	MCA Busy Out
8	BSYIN	Device Busy In
9	COLLECT	Status Out
10	I/O	Status Out
11	STOPCOL	Stop Collect In
12	STARTCOL	Start Collect In
13	CLRDAT	Clear Data In
15	GATE	Gate In
21	AMS	Abort MCS Sweep In
22	AOF	Address Overflow (MCS end of sweep)
23	GND	Ground
24	GND	Ground
25	STARTIO	Start Readout In

A.11.10 J113, J114, 115-External ADC Connectors

See Section 9.3.6 for signals.

A.11.11 J116, J118-PUR/LTC Connectors

Pin	Signal	Description	To Mother Board
J116 1	LG	Linear Gate Out	G (1A-33)
2	REJ	Reject In	E (1A-92)
3	GND	Ground	A —
J118 BNC	ADCBUSY	Busy In	W (1A-75
J118	GND	Ground	Z —

Appendix B
Field Installation Instructions

B.1 INTRODUCTION

The Monitor (CRT Assembly) and individual boards can be removed or replaced by following the appropriate instructions included in this manual. Also included are detailed instructions for Field Installation of any options which may be purchased at a later time.

B.1.1 COVER REMOVAL

Before attempting to remove the covers, turn off the ac power and remove the ac line cord from the rear of the Analyzer.

To remove the top and bottom covers, simply remove the four (4) black Phillips-head screws from each side of the covers, lift off the top cover, and lift the Analyzer out of the bottom cover. After replacing a board or installing an option, reconnect the ac line cord to the Analyzer, turn on the ac power and check the operation of the unit before replacing the covers.

If any question arises during the installation or the operational check-out, please contact your local Canberra Representative or Canberra's Customer Service Department.

B.1.2 BOARD REMOVAL AND REPLACEMENT

The Printed Circuit (PC) Boards may be removed from the Analyzer by applying equal pressure to the card ejectors at each end of the board and pulling up.

The boards are installed by aligning the board in the card guide slots mounted on the front and back of the card cage and sliding the board all the way down. Press the board firmly down into the Mother Board socket, flexing the board if necessary to align it with the socket. Be sure the board is firmly seated in the Mother Board socket.

The cable entry opening shown at the rear of the Monitor compartment (see Figure B-1) is used to pass the wiring of various options from the rear panel connectors to the Mother Board edge connectors.

B.1.3 FIRMWARE UPDATE

To change the basic Firmware set to a later version, all plug-in chips (PROMs) on the CPU Board (except A45, the Microprocessor), including any option chips, must be updated to the same Firmware revision level to allow proper operation of the Analyzer.

1. Remove the CPU Board from the Analyzer.
2. Using a small screwdriver or an LSI chip-puller, carefully remove the 16 chips is sockets A12 - A15, A28 - A31, A50 - A53, and A64 - A67. (See Figure B-4 for socket locations.)
3. Insert the chips of the new Firmware set into the socket named on each chip's label.

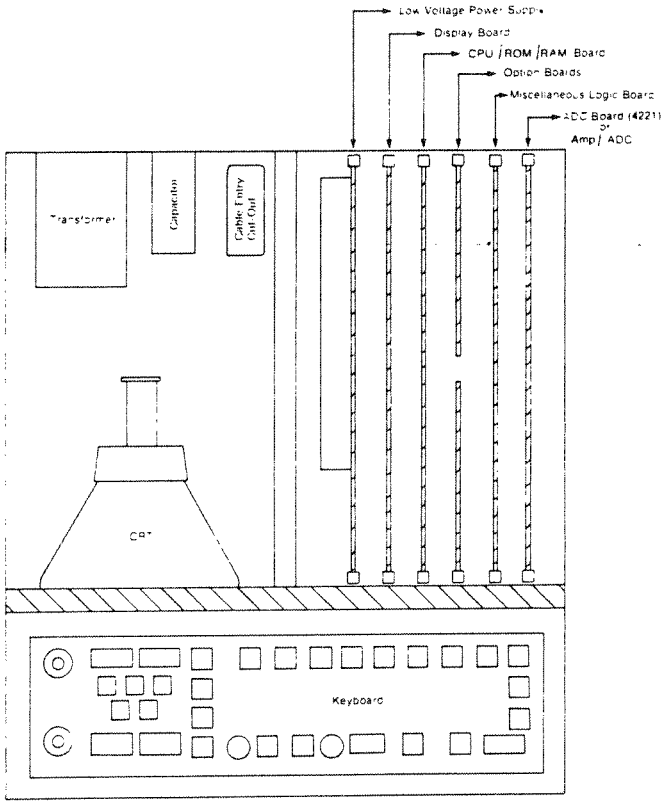
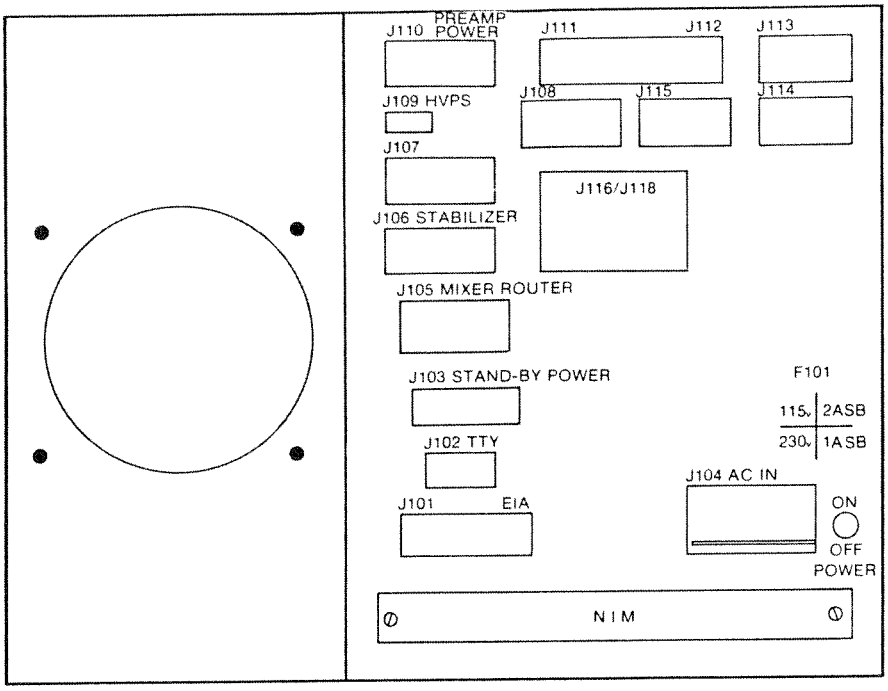


Figure B-1
Series 40
Board Locations



Location	Designation
J101	EIA Connector
J102	Teletype Connector
J103	Stand-by Power Supply
J104	AC Line Input
J105	Mixer Router
J106	Stabilizer Data/External ADC 1
J107/J108	I/O Options
J109	High Voltage Power Supply
J110	Preamplifier Power Supply
J111/J112	Option 4222/4232
J113/J114/J115	ADC Multiplexer Inputs
J116/J118	Pile-up Rejector

Figure B-2
Series 40 Rear Panel

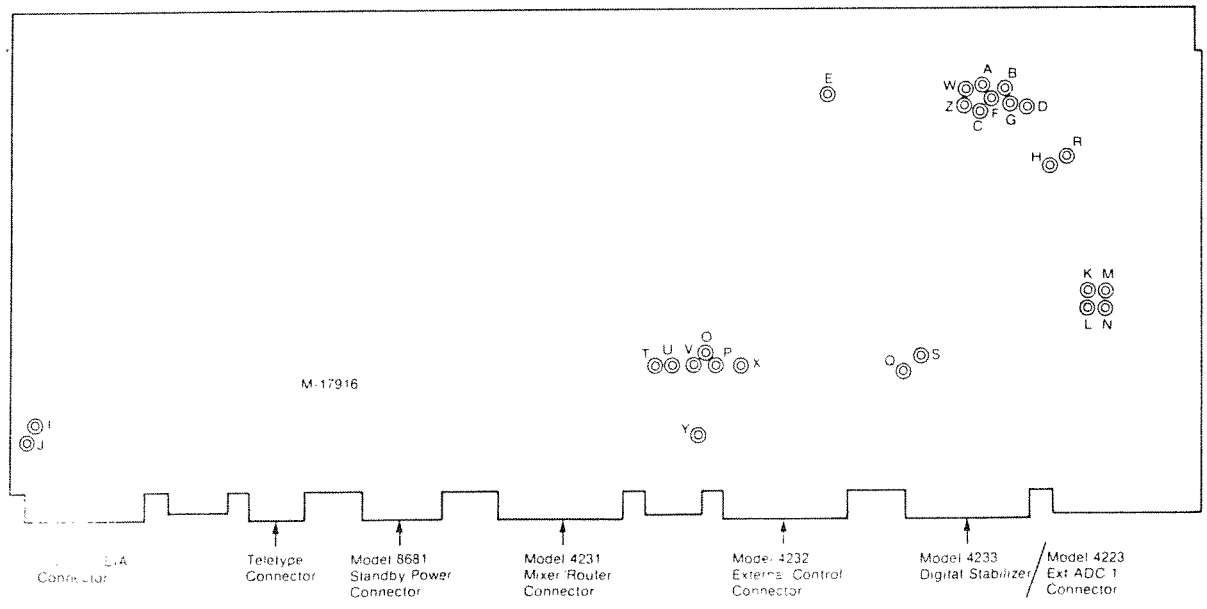


Figure B-3
Mother Board - Bottom View

When inserting a chip, take care to insert it firmly into the socket without bending any pins under the chip or leaving any pins outside of the socket. Be sure that the chip is plugged in with the notch in the chip toward the top of the board; the socket has a notch at the top as a guide (see Figure B-4).

CAUTION:
Inserting a chip reversed will cause permanent damage to the chip when power is applied. Be certain that all chips are inserted correctly before replacing the CPU Board in the Analyzer.

4. Replace the CPU Board in the Analyzer.
5. If the new Firmware is being installed in a Model 4203 (8K Channel) Analyzer, which currently has version 2.1, remove the Display Board from the Analyzer. Remove chip A44, which is marked with two green dots (see Figure B-5), and replace it with the supplied new chip marked with two red dots. Replace the Display Board in the Analyzer.
6. Before replacing the covers, check the Analyzer for proper operation.
7. On power up, check Firmware version number displayed (see Figure B-6) to verify that the correct Firmware set has been installed.

B.1.4 MONITOR REPLACEMENT

The Monitor Assembly can be removed by pulling the connector off of the rear of the Monitor Assembly printed circuit board and removing the four (4) screws, one in each corner of the bottom of the Monitor frame. A Phillips screwdriver with a 23 cm (9 in.) shank will make removal of the screws easier.

The Model 4262 Service Kit kncludes the 23 cm Phillips screwdriver and other useful servicing aids.

Pull the Monitor slightly to the rear and carefully lift it straight up and out of the Analyzer. Some Monitors will require that the Analyzer's front panel be dropped first: remove two (2) screws on each side of and three (3) screws on the top of the front panel.

To reinstall the Monitor, reverse the removal procedure. Be sure that the wiring connector is seated securely on the printed circuit board edge connector and the four (4) screws are tightened down.

B.1.5 FIELD INSTALLATION OF OPTIONS

After removing the covers (see Section B.1.1), proceed to the appropriate section for the option being installed. Before replacing the covers, check the operation of the option.

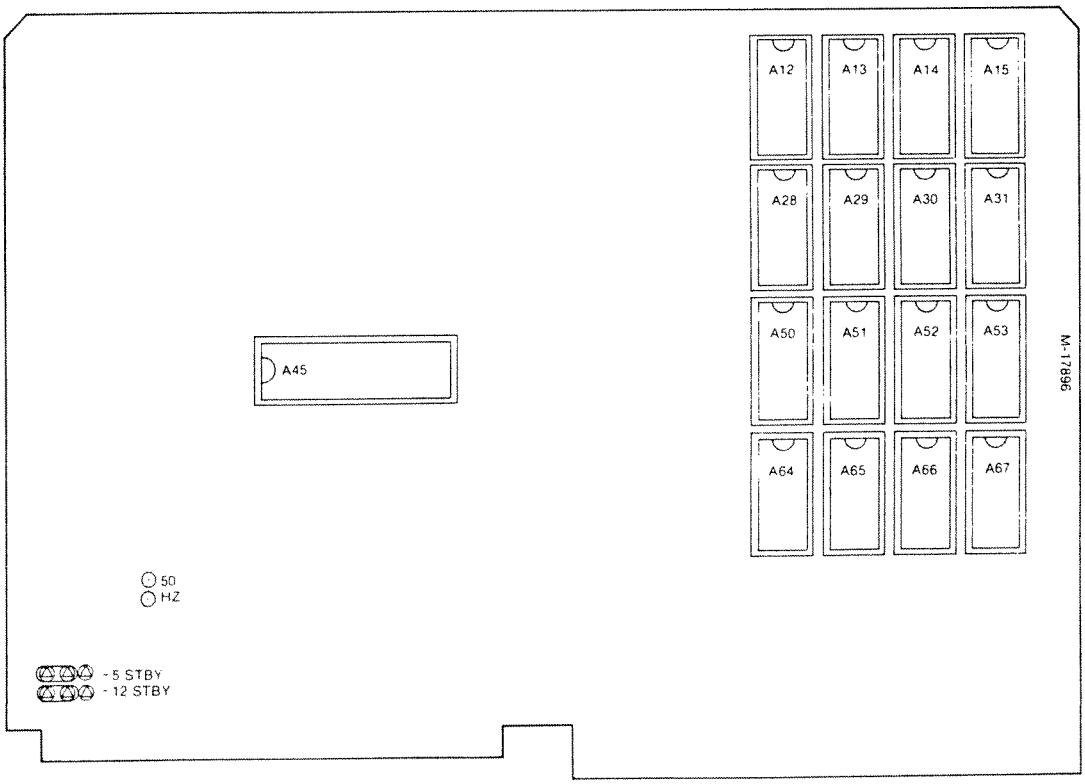


Figure B-4
CPU Board

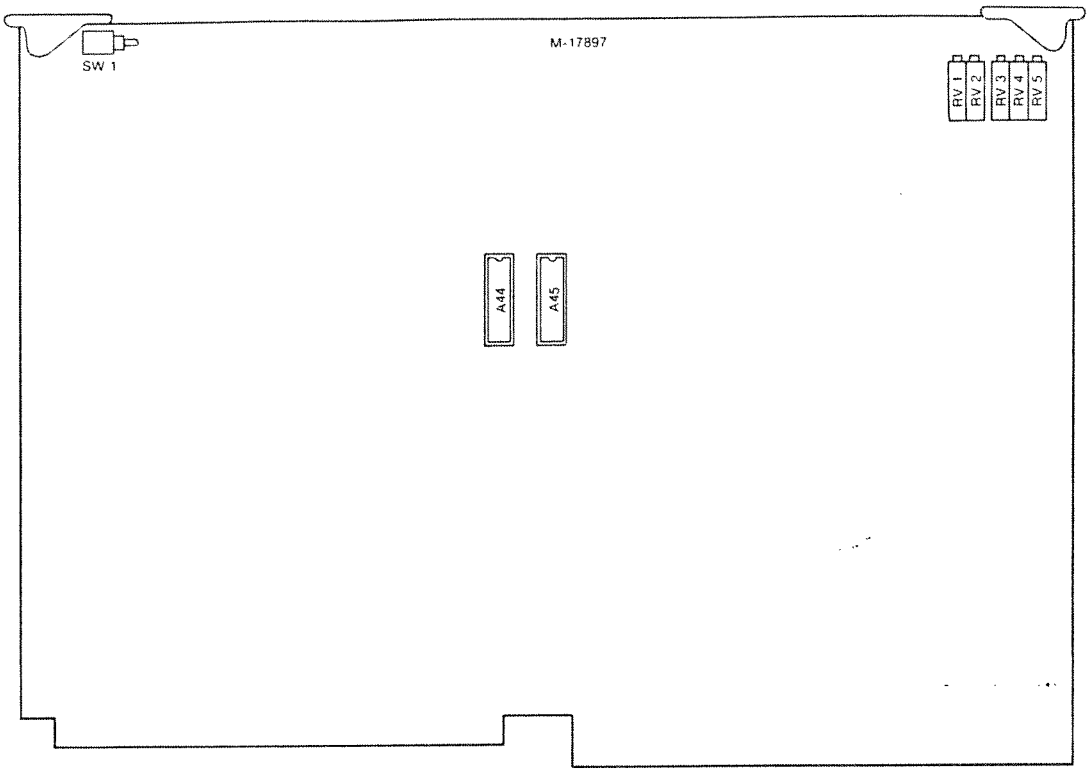


Figure B-5
Display Board

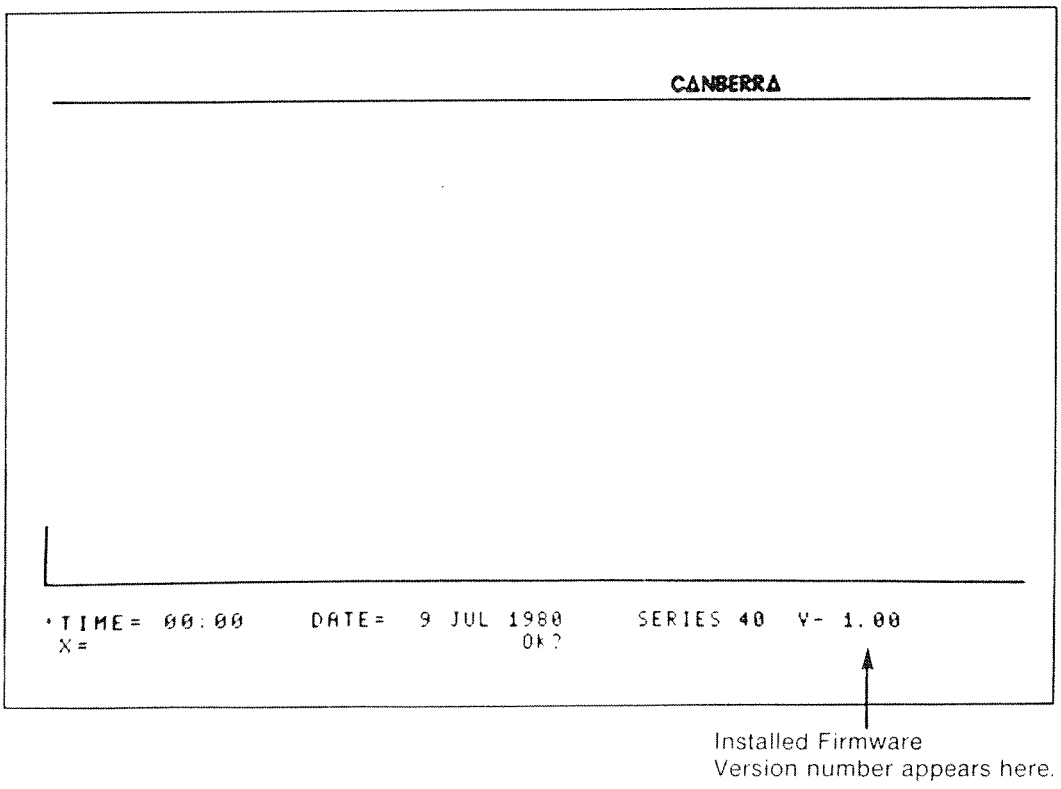


Figure B-6
Display at Power On

When Installing options that have a D-type male connector to be mounted on the Analyzer's rear panel, be sure to mount the connector narrow side down.

Figure B-7
Connector Orientation

B.2 MODEL 4222 HIGH-PERFORMANCE MCS OPTION

This option consists of a small plug-in printed circuit (PC) board. It also requires the Model 4232 External Control Wiring.

1. Remove the Miscellaneous Logic Board from the Analyzer.
2. Plug the small PC board into J1, the connector at the top right corner of the Miscellaneous Logic Board.
3. Replace the Miscellaneous Logic Board in the Analyzer.
4. See Section B-5 for the Model 4232 installation instructions.
5. Before replacing the Analyzer's covers, check the installation for proper operation.

B.3 MODEL 4223 MULTI—ADC INTERFACE

The Model 4223 Interface is to be installed in an Analyzer that has Firmware version 2.2, or later, installed. The Firmware version can be determined at power on (see Figure B-6). If the Analyzer's Firmware version is earlier than 2.2, contact your local Canberra Representative or Canberra's Customer Service Department.

The Model 4223 Interface consists of the Multi-ADC Interface Board, with three (3) ribbon cables attached to it, and a single separate ribbon cable. To install the interface:

1. Remove the cover plates from the Analyzer's rear panel, which are marked J113, J114, J115, and J106 (see Figure B-2).
2. Remove the cables from J1, J2, and J3 on the ADC Board.
3. Remove the ADC Board from the Analyzer.
4. Insert the Model 4223 Interface Board in its place.
5. Install the three attached ribbon cables, as marked, in J113, J114, and J115.
6. Install the separate ribbon cable in J106.
7. Fasten the connectors in place with the hardware supplied with the option.

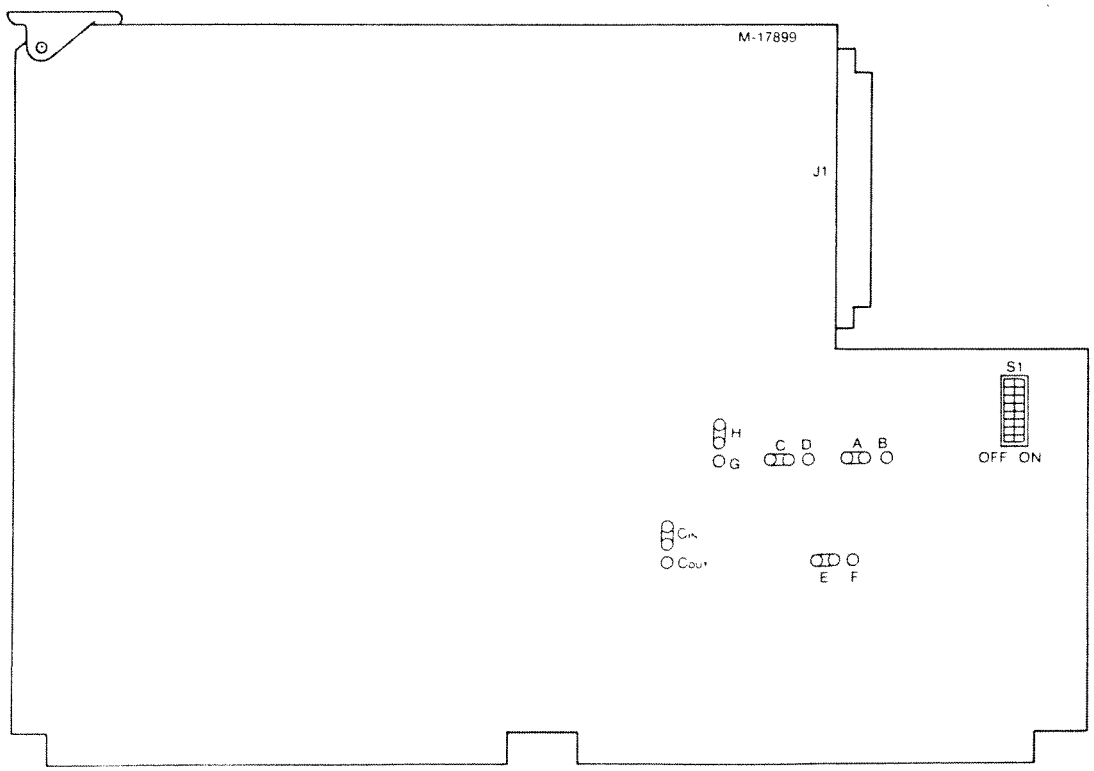


Figure B-8
Miscellaneous Logic Board

8. Dress the three ribbon cables attached to the board across the back of the boards and place any cable slack inside the Monitor compartment.
9. Carefully route the single separate ribbon cable (from J106) through the cable entry opening at the bottom right rear of the Monitor compartment.
10. Connect the three cables removed from the ADC Board to the mating connectors on the Interface Board.
11. Turn the Analyzer over. Remove the three nuts holding the cable retaining bracket and remove the bracket. On earlier Series 40s, there is no retaining bracket.
12. Plug the plastic connector on the cable onto the rear-most edge connector, marked Stabilizer, of the Mother Board (see Figure 3) with the blue stripe on the cable to the right.
13. Reinstall the cable retaining bracket and its three nuts.
14. Turn the Analyzer right side up and remove the Miscellaneous Logic Board.
15. Change jumper "H" to position "G" on the Miscellaneous Logic Board (see Figure B-8).
16. Before replacing the covers on the Analyzer, check the installation for proper operation.

B.4 MODEL 4231A MIXER/ROUTER WIRING

The Model 4231A Wiring option consists of a ribbon cable with a 25-pin, D-type connector at one end and a plastic edge connector at the other end, and three DIP jumper plugs.

1. Remove the cover plate on the panel of the Analyzer, marked J105 (see Figure B-2).
2. Mount the Model 4231 connector in the J105 opening and fasten it is place with the hardware supplied with the option.
3. Carefully route the ribbon cable through the cable entry opening at the bottom right rear of the Monitor compartment (see Figure 1).
4. Turn the Analyzer over. Remove the three nuts holding the cable retaining bracket and remove the bracket. On earlier Series 40s, there is no retaining bracket.
5. Plug the plastic connector into the Mixer/Router edge connector on the Mother Board (see Figure B-3) with the blue stripe on the cable to the right.
6. Reinstall the cable retaining bracket and its three nuts.
7. Turn the Analyzer right side up, remove the three cables at J1, J2, and J3 on the ADC Board and remove the ADC Board from the Analyzer.
8. Install one of the DIP jumper plugs in J7 on early ADC Boards (see Figure B-10a) or in A52 on Revision G or later ADC Boards (see Figure B-10b). The plug used must match the Analyzer's memory size.

For a Model # :	Use the plug marked:
4201	High Perf. 1K
4202	High Perf. 4K
4203	High Perf. 8K

Be sure to insert the plug with the pin 1 marking at the top of the socket. Take care to ensure that no plug pins are left outside of the socket or bent under the plug. If all pins are not in the socket, improper operation may result.

9. Replace the ADC Board in the Analyzer and reconnect the Analyzer's three cables to J1, J2, and J3 on the ADC Board.
10. Remove the Miscellaneous Logic Board from the Analyzer, change jumper "H" to position "G" for the Model 8222. For the Models 8222A/B, use position H (see Figure B-8 for jumper location). Replace the board in the Analyzer.
11. Before replacing the Analyzer's covers, check the installation for proper operation.

B.5 MODEL 4232 EXTERNAL CONTROL WIRING

The Model 4232 Wiring option consists of a ribbon cable with a 25-pin, D-type connector at one end and a plastic edge connector at the other end, a twisted pair cable attached to the connector plate, which is terminated in push-on connectors.

1. Remove the cover plate on the large connector opening at the top center of the Analyzer's rear panel. (J111 - J112 in Figure B.2).
2. Mount the Model 4232 connector plate inside the rear panel and fasten it in place with the screws and nuts removed with the blank cover plate.
3. Carefully route the ribbon cable and the twisted pair cable through the cable entry opening at the bottom right rear of the Monitor compartment.
4. Turn the Analyzer over. Remove the three nuts holding the cable retaining bracket and remove the bracket. On earlier Series 40s, there is no retaining bracket.
5. Plug the plastic connector onto the External Control edge connector on the Mother Board (see Figure B-3) with the blue stripe on the cable to the right.
6. Replace the cable retaining bracket and its three nuts.
7. Plug the red wire in the twisted pair cable onto the pin at terminal H on the Mother Board.
8. Plug the black wire in the twisted pair cable onto the pin at terminal R on the Mother Board.

The twisted pair cable connects the MCS Count Input to the High Performance MCS Board (Model 4222). If this option is to be installed, note that there is provision on the Miscellaneous Logic Board for a terminating resistor at the High Performance receiving circuit.

The terminating resistor doesn't need to be installed unless a cable greater than 3 m (10 ft.) in length is to be connected to the MCS Count Input. The purpose of the terminating resistor for long cables is to prevent false counting caused by signal reflections due to cable termination mismatch.

If a long cable is to be used at the MCS Count Input, install a resistor that matches the impedance of the signal cable. The resistor is installed on the Miscellaneous Logic Board in sockets L and M (next to A14) at the upper left side of the board.

Before replacing the Analyzer's covers, check the installation for proper operation.

B.6 MODEL 4233 DIGITAL STABILIZER WIRING

The Model 4233 Wiring option consists of a ribbon cable with a 25-pin D-type connector at one end and a plastic edge connector at the other end.

If the option is to be used with an older Model 8200 Stablilzer, two timing capacitors, located on the Stabilizer's Control Logic Board (PC 1) will have to be changed (see Figure B-9):

C9 (on P16, pins 10 and 11) to 82 pF, NPO type capacitor
C11 (on P15, pins 10 and 11) to 22 pF

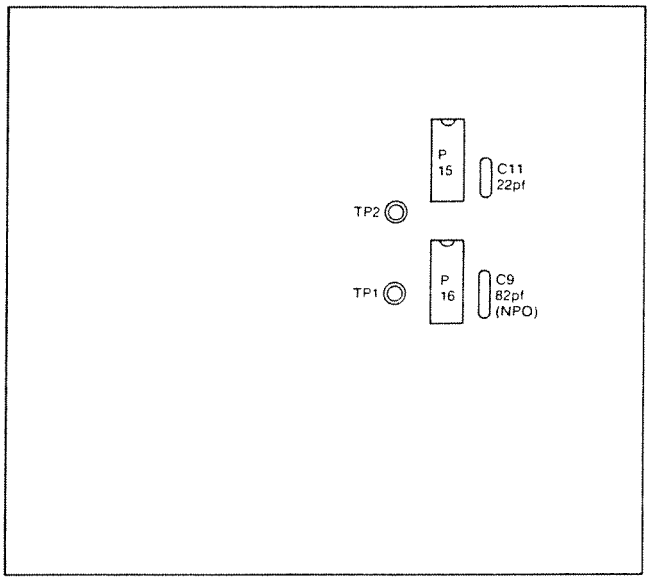
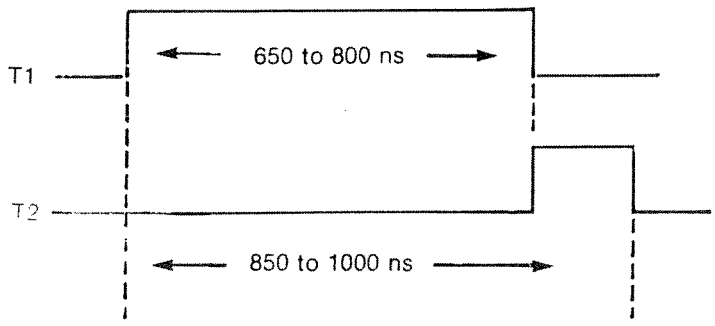


Figure B-9
Model 8200 - PC1

With these capacitors installed, the following timing pulses should be seen at Test Points 1 and 2 (see Figure B-9):



On a Model 8200 shipped with the Series 40, the timing capacitors will have been changed at the factory.

To install the cable:

1. Remove the cover plate on the rear panel of the Analyzer, marked J106 (see Figure B-2).
2. Mount the Model 4233 connector in the J106 opening and fasten it in place with the hardware supplied with the option.
3. Carefully route the ribbon cable through the cable entry opening at the bottom right rear of the Monitor compartment.
4. Turn the Analyzer over. Remove the three nuts holding the cable retaining bracket and remove the bracket. Early Series 40s do not have the retaining bracket.
5. Plug the plastic connector onto the Stabilizer edge connector on the Mother Board (see Figure B-3) with the blue stripe on the cable to the right.
6. Replace the cable retaining bracket and its three nuts.
7. Turn the Analyzer right side up and connect the Model 8200 Stabilizer to J106 with the 25-pin cable supplied with the Stabilizer.

   NOTE: Early Stabilizers used a 24-pin connector which will require an adapter cable.

   An adapter cable may be ordered from the factory, assembled and tested, or may be made in the field by referring to Section 8.3.3 of this Manual.

8. Before replacing the covers, check the installation for proper operation. Refer to the Model 8200 Manual for instructions on its operation.

B.7 MODEL 4234 PUR/LTC WIRING

The Model 4234 Wiring option consists of a five-wire harness and an external cable.

1. Remove the large blank cover plate (J116/J118 in Figure B-2) located on the Analyzer's rear panel just under the connector locations marked J108 and J115.
2. Mount the Model 4234 connector plate inside the rear panel and fasten it in pla· ·with the screws and nuts re.noved with the blank cover plate.
3. Carefully route the wire harness through the cable entry opening at the bottom right rear of the Monitor compartment.
4. Turn the Analyzer over and plug the harness wires onto the designated pins on the Mother Board (see Figure B-3):

   The twisted pair in the harness plug onto:
   Red to pin W
   Black to pin Z

   The remaining three wires plug onto:
   Green to pin G
   Yellow to pin E
   Black to pin A

5. Turn the Analyzer right side up and remove the three cables from J1, J2, and J3 on the ADC Board.
6. Remove the ADC Board from the Analyzer and check the Revision designation of the board. This is the letter found after the M-17934 designation at the bottom of the component side of the board (see Figure B-10).
7. If the board's revision level is "C", a modification will have to be made to the ADC Board to assure proper PUR/LTC operation (see Section B.7.1)
8. If the revision level is "-D" or later, replace the board in the Analyzer and reconnect the three cables to J1, J2, and J3.
9. Before replacing the covers on the Analyzer, check the installation for proper operation.

B.7.1 ADC BOARD MODIFICATION

With the ADC Board (Revision C only) removed from the Analyzer:

1. Disconnect A9, pin 8 from A18, pin 5.
2. Connect A18, pin 5 to A18, pin 4.
3. Connect the cathode of a 1N995 diode to A9, pin 8.
4. Connect the anode of the 1N995 diode to A23, pin 11.
5. Be certain that there is no excess solder or flux left on the connections to prevent possible circuit malfunction.
6. Replace the ADC Board in the Analyzer and reconnect the three cables to J1, J2, and J3.
7. Before replacing the covers on the Analyzer, check the installation for proper operation.

B.8 MODELS 4241 DEFINE/USE/AP-PAK and 4242 LEARN/EXECUTE OPTIONS

The Models 4241 and 4242 Analysis options consist of programmed integrated circuits (chips). The chips are labeled with the Model number, the Firmware version, and a socket number.

The Firmware version number on the chips must match the Firmware version installed in the Analyzer. The Analyzer's Firmware version may be determined at power on (see Figure B-6). If the two Firmware version numbers do not match, consult your local Canberra Representative or Canberra's Customer Service Department.

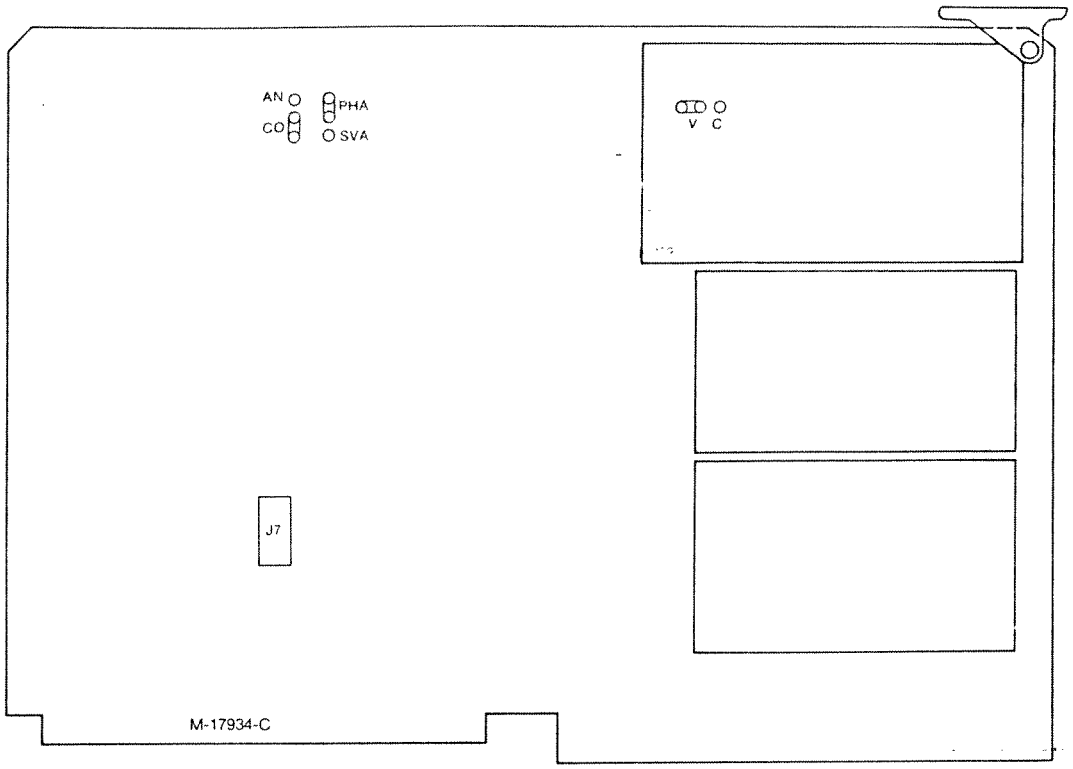


Figure B-10a
Early ADC Board

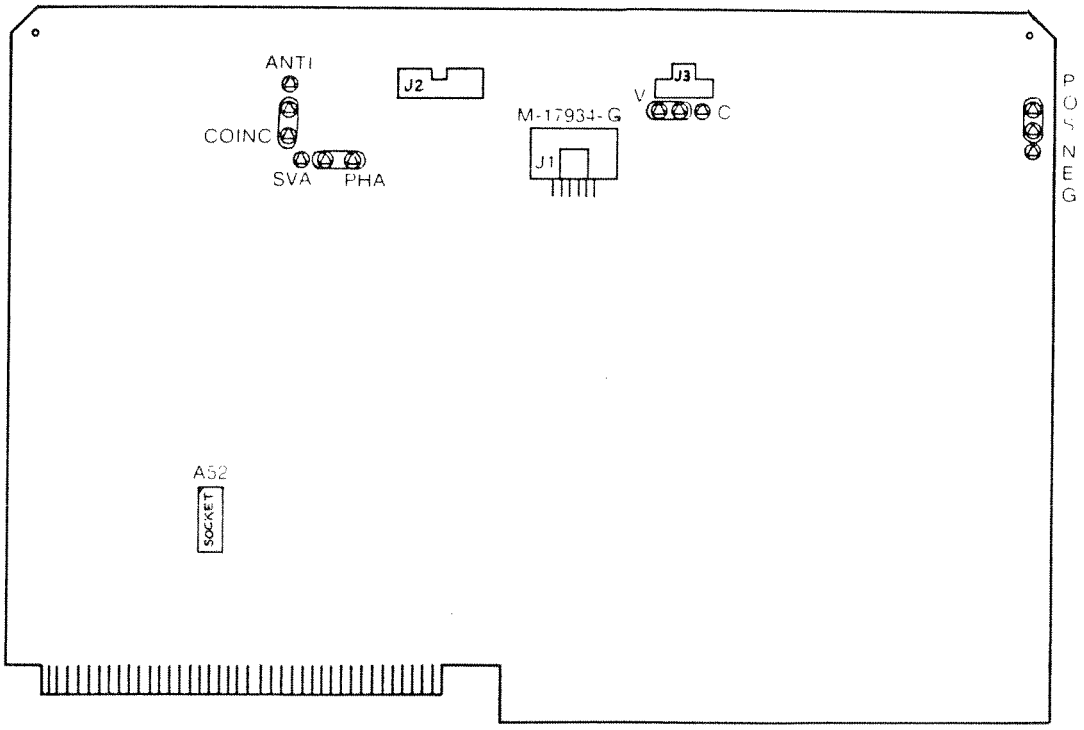


Figure B-10b
Revision G ADC Board

With Firmware version 2.1, each of these options is on a single chip; the Models 4241 and 4273 are mutually exclusive - only one of these two can be installed in the Analyzer.

With Firmware version 2.2 and later, the Models 4241 and 4242 are on more than one chip; both may be installed with either the Model 4273 or the Model 4273A.

With any Firmware version, the Model 4242 Learn/Execute will replace the existing "Recycle" chip.

To install either option:

1. Remove the CPU Board from the Analyzer.
2. Locate the socket number indicated on the chip (see Figure B.4 for location).
3. If the Model 4242 is being installed, remove the "Recycle" chip from the CPU Board.
4. Install the chip (or chips) in the correct CPU Board socket.

When inserting a chip, take care to insert it firmly into the socket without bending any pins under the chip or leaving any pins outside the socket. Be sure that the chip is plugged in with the notch in the chip towards the top of the board; the socket has a notch at the top as a guide.

CAUTION: Inserting a chip reversed will cause permanent damage to the chip when power is applied. Be certain the chip is inserted correctly before replacing the board in the Analyzer.

5. Replace the board in the Analyzer.
6. Before replacing the covers on the Analyzer, check the installation for proper operation.

B.9 MODEL 4251 X-Y PLOTTER INTERFACE

The Model 4251 Interface consists of: a printed circuit board with an attached cable which is terminated in a connector; an identifying decal; and a programmed integrated circuit (chip) marked with the Model number, the Firmware version and a socket number. The interconnecting cable is attached to the Houston Plotter (Canberra Model 5201). The cable for any other plotter must be ordered separately.

The Firmware version number on the chip must match the Firmware installed in the Analyzer. The Analyzer's Firmware version may be determined at power on (see Figure B-6).

If the two Firmware versions do not match, consult your local Canberra Representative or Canberra's Customer Service Department.

With Firmware version 2.1 or earlier, the Model 4251 Interface is mutually exclusive with the Model 4253 Graphics Plotter Interface - only one of the two may be installed in the Analyzer. Version 2.1 Firmware includes the X-Y Plotter program chip in the basic Firmware set; only the Interface Board needs to be installed in the Analyzer.

With Firmware version 2.2, both the Model 4251 and 4253 may be installed in the same Analyzer.

With Firmware version 2.3 or later, Models 4251, 4252 and 4253 are mutually exclusive - only one of these may be installed.

These later versions on the Firmware do not contain the Plotter program chip; both the Interface Board and the chip must be installed in the Analyzer.

Before installing the Interface Board in the Analyzer, check the two jumpers on the board to verify that they are in positions B-C and E-F (see Section A.7 of this Manual for jumper functions).

1. Remove the rear panel plate which covers the opening marked J107 (or J108). See Figure B-2.
2. Install the Interface Board in either of the two I/O slots in the Analyzer's Mother Board (see Figure B-1).
3. Install the cable attached to the board in the opening at J107 (or J108) on the Analyzer's rear panel.
4. Fasten the connector in place with the hardware supplied with the Interface.
5. Apply the supplied identifying decal to the rear panel connector location.
6. Dress the connector cable across the back of the boards and place any cable slack inside the Monitor compartment.

If the Analyzer has Firmware version 2.1 installed, go on to step 11.

7. Remove the CPU Board from the Analyzer.
8. Locate the socket number indicated on the chip (see Figure B-4 for locations).
9. Install the chip in the correct CPU Board location.

When inserting the chip, take care to insert it firmly into the socket without bending any pins under the chip or leaving any pins outside the socket. Be sure that the chip is plugged in with the notch in the chip toward the top of the board; the socket has a notch at the top as a guide.

CAUTION: Inserting a chip reversed will cause permanent damage to the chip when power is applied. Be certain that the chip is inserted correctly before replacing the board in the Analyzer.

10. Replace the board in the Analyzer.
11. Before replacing the covers on the Analyzer, check the installation for proper operation.

B.10 MODEL 4252 PRINTER/PLOTTER INTERFACE

Models 4251, 4252, and 4253 are mutually exclusive - only one of these may be installed in the Analyzer.

The Model 4252 Interface consists of; a printed circuit board with an attached cable terminated in a 25-pin connector; an identifying decal; an interconnecting cable; and a programmed integrated circuit (chip) marked with the Model number, the Firmware version and a socket number.

Before installing the Interface Board in the Analyzer, check that the jumpers and switch positions are set correctly. Refer to Figure B-11.

52/53/73 jumper in the 52 position
C-D jumper in the D position
H-I jumper in the I position

With the M-N jumper out or in the N position, control characters (CTL) will be transmitted with the data. With a jumper in the M position, CTL will be inhibited.

DIP Switch (A32, lower right section of the board) set to:

Switch	Position	Comment
1	OFF	
2	OFF	Switches 1 - 4 set for
3	OFF	19.2k Baud
4	OFF	
5	OFF	8 characters
6	ON	Disables Parity
7	OFF	Even Parity
8	ON	One Stop Bit

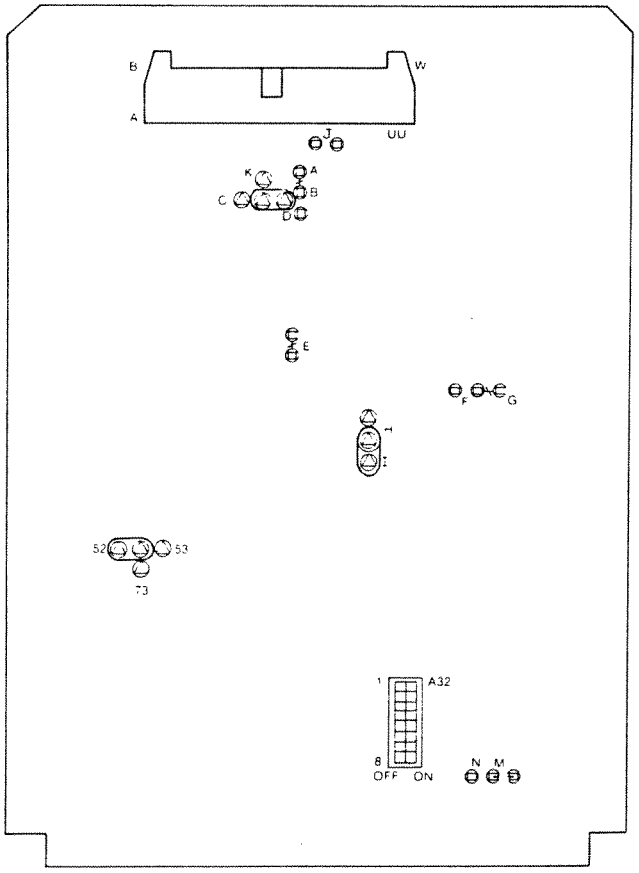


Figure B-11
Model 4252 Printer/Plotter Interface Board

B.11 MODEL 4253 GRAPHICS PLOTTER INTERFACE

The Model 4253 Interface consists of; a printed circuit board with an attached cable terminated in a 25-pin connector; an identifying decal; an interconnecting cable; and a programmed integrated circuit (chip) marked with the Model number, the Firmware version and a socket number.

The Firmware version number on the chip must match the Firmware version installed in the Analyzer. The Analyzer's Firmware version may be determined at power on (see Figure B-6). If the two Firmware version numbers do not match, consult your local Canberra Representative or Canberra's Customer Service Department.

With Firmware version 2.1 or earlier, the Model 4253 is mutually exclusive with the Model 4251 X-Y Plotter Interface - only one of the two may be installed in the Analyzer. With Firmware version 2.2, both may be installed in the Analyzer.

With Firmware version 2.3 or later, Models 4251, 4252, and 4253 are mutually exclusive - only one of these may be installed.

Before installing the Interface Board in the Analyzer, check that the jumpers and switch positions are set correctly:

52/53/73 jumper in the 53 position
C-D jumper in the D position
H-I jumper in the I position
M-N jumper out or in the N position for line plot (this jumper is not included on early Interface Boards)
M-N jumper in the M position for point plot (Firmware version 2.4 or later only).

DIP Switch (A32, lower right section of the board) set to:

Switch	Position	Comment
1	ON	
2	OFF	Switches 1 - 4 set for
3	ON	2400 Baud
4	OFF	
5	ON	8 characters
6	ON	Disable Parity
7	ANY	Not Applicable
8	OFF	Two Stop Bits

To Install the option:

1. Remove the rear panel plate which covers the opening marked J107 (or J108). See Figure B-2.
2. Install the Interface Board in either of the two I/O slots in the Analyzer-s Mother Board (see Figure B-1).
3. Install the cable attached to the board in the opening at J107 (or J108) on the Analyzer's rear panel.
4. Fasten the connector in place with the hardware supplied with the option.
5. Apply the supplied identifying decal to the rear panel connector location.
6. Dress the connector cable across the back of the boards and place any cable slack inside the Monitor compartment.
7. Remove the CPU Board from the Analyzer (see Figure B-1).
8. Locate the socket number marked on the chip (see Figure B-4 for location).
9. Install the chip in the correct CPU Board location.

When inserting the chip, take care to insert it firmly into the socket without bending any pins under the chip or leaving any pins outside of the socket. Be sure that the chip is plugged in with the notch in the chip toward the top of the board; the socket has a notch at the top as a guide.

CAUTION: Inserting the chip reversed will cause permanent damage to the chip when power is applied. Be certain that the chip is inserted correctly before replacing the board in the Analyzer.

NOTE: In Analyzers with version 2.1 Firmware, the chip in location A53 will have to be removed before inserting the option chip. In Analyzers with later Firmware versions, insert the chip in the socket Marked on the chip.

10. Replace the CPU Board in the Analyzer.
11. Before replacing the covers on the Analyzer, check the installation for proper operation.

B.12 MODEL 4254 MAGNETIC TAPE INTERFACE

The Model 4254 Interface consists of: a printed circuit board, a cable terminated in a 25-pin connector and a flat plastic connector; an identifying decal, an interconnecting cable; and a programmed integrated circuit (chip) marked with the Model number, the Firmware version and a socket number.

The Firmware version number on the chip must match the Firmware version installed in the Analyzer. The Analyzer's Firmware version may be determined at power on (see Figure B-6). If the two Firmware version numbers do not match, consult your local Canberra Representative or Canberra's Customer Service Department.

Before installing the Interface Board in the Analyzer, check that the jumpers are set correctly. Refer to Figure B.12.

The factory settings are: A-B, E-F, H-I, K-L, Y-Z, 2716. Appendix A.9 details the use of other jumper positions.

To Install the option:

1. Remove the rear panel plate which covers the opening marked J107 (or J108). See Figure B-2.
2. Install the Interface Board in the rear I/O slot in the Analyzer's Mother Board (see Figure B-1). If there already is an EIA board in this slot, pull it out and move it to the front I/O slot.
3. Plug the board's cable into the socket at the top of the board and install the 25-pin connector in the opening at J107 (or J108) on the Analyzer's rear panel.
4. Fasten the connector in place with the hardware supplied with the option.
5. Apply the supplied identifying decal to the rear panel connector location.
6. Dress the connector cable across the back of the boards and place any cable slack inside the Monitor compartment.
7. Remove the CPU Board from the Analyzer.
8. Locate the socket number marked on the chip (see Figure B-4 for location).
9. Install the chip in the correct CPU Board location.

When inserting the chip, take care to insert it firmly into the socket without bending any pins under the chip or leaving any pins outside of the socket. Be sure that the chip is plugged in with the notch in the chip toward the top of the board; the socket has a notch at the top as a guide.

CAUTION: Inserting the chip reversed will cause permanent damage to the chip when power is applied. Be certain that the chip is inserted correctly before replacing the board in the Analyzer.

10. Replace the CPU Board in the Analyzer.
11. Remove the display board and modify it as described in section B.12.1.
12. Replace the display board in the Analyzer.
13. Before replacing the covers on the Analyzer, check the installation for proper operation.

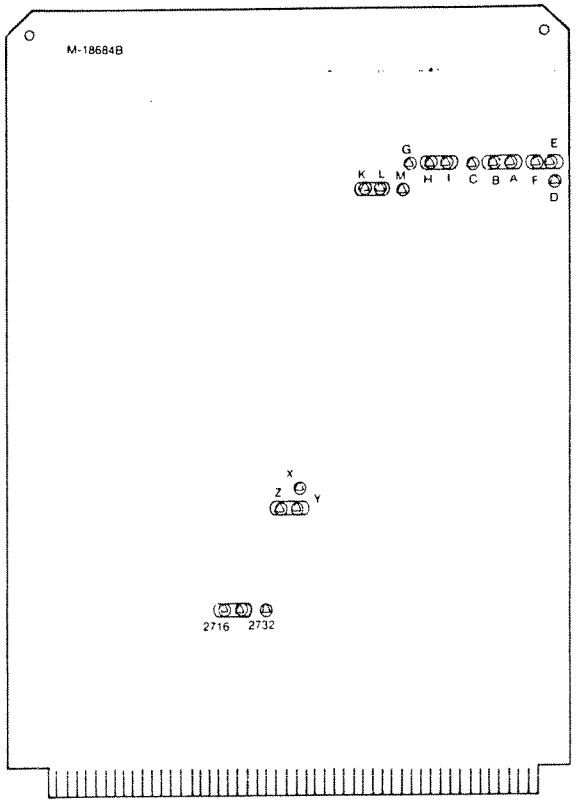
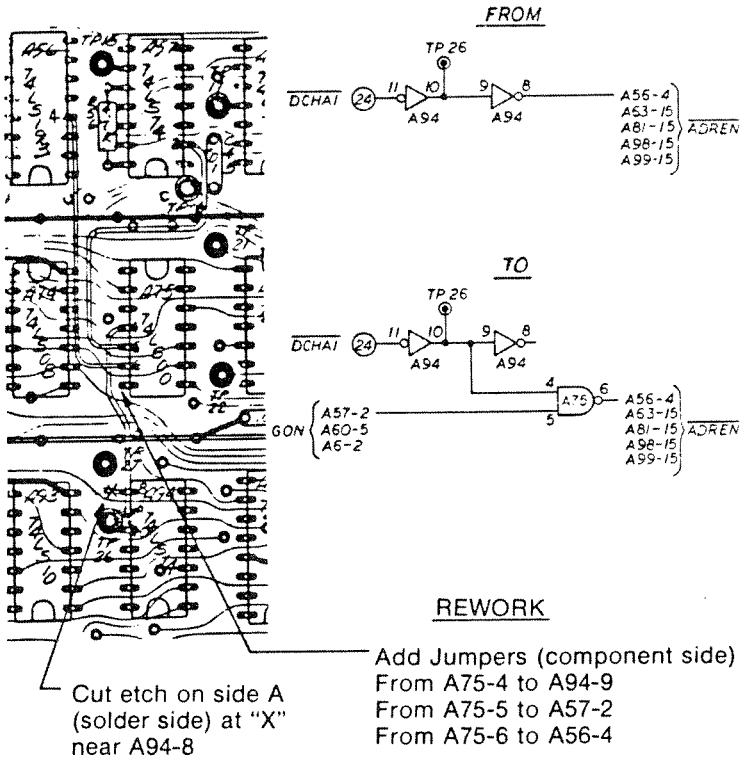


Figure B-12
Magnetic Tape Interface

B.12.1 DISPLAY BOARD MODIFICATION

Signal DCHAI causes data bus conflict between the Video Display Board and Series 40 Magnetic Tape Interface Board.

To install logic to disable the Video Display Board response to DCHAI while Mag Tape Interface is requesting the data bus, do the following rework per AR 11316.



To Install the option:

1. Remove the cover plate from J107 (or J108) on the Analyzer's rear panel (see Figure B-2).
2. Install the Interface Board in one of the Option Board slots (see Figure B-1).
3. Mount the ribbon-cable connector on the rear panel with the two supplied jackscrews and tighten the jackscrews firmly.
4. Fold about 5 cm (2 in.) of the cable down on the right side of the Interface Board (looking from the front of the unit). This will prevent the cable connector from pulling out of the board's socket.
5. Pass the rest of the cable across the top of the other boards to the left. Place any slack in the cable inside the Monitor compartment.
6. Place the supplied identifying decal to the rear panel connector location.
7. Before replacing the cover, check the installation for proper operation.

When inserting the chip, take care to insert it firmly into the socket without bending any pins under the chip or leaving any pins outside of the socket. Be sure that the chip is plugged in with the notch in the chip toward the top of the board; the socket has a notch at the top as a guide.

CAUTION: Inserting the chip reversed will cause permanent damage to the chip when power is applied. Be certain that the chip is inserted correctly before replacing the board in the Analyzer.

10. Replace the CPU Board in the Analyzer.
11. Before replacing the covers on the Analyzer, chec the installation for proper operation.

B.13 MODEL 4271 COMPUTER INTERRFACE

The Model 4271, 4272, and 4273 are mutually exclusive - only one of these can be installed in the Analyzer.

The Model 4271 Computer Interface includes: a printed circuit board with an attached cable which is terminated in a 25-pin connector; a programmed integrated circuit (chip) marked with the Model number, the Firmware version number and a socket number; and an identifying decal.

The Firmware version number on the chip must match the Firmware installed in the Analyzer. The Analyzer's Firmware version may be determined at power on (see Figure B-6).

If the two Firmware version numbers do not match, consult your local Canberra Representative or Canberra's Customer Service Department.

Before installing the Interface Board in the Analyzer, check that the jumpers and switch positions are set correctly. (see Figure B-13):

52/53/73 jumper in the 73 position.
C-D jumper in the D position for RSX-11 systems, or in the K position for RT-11 systems.
H-I jumper in the H position.
M-N jumper out (not used with Model 4271).

DIP switch (A32) set to:

Switch	Position	Comment
1	ON	Switches 1-4 Set for 9600 Baud
2	OFF	
3	OFF	
4	OFF	
5	OFF	8 Characters
6	OFF	Enables Parity
7	OFF	Even Parity
8	ON	One Stop Bit

To install the option:

1. Remove the rear panel plate which covers the opening marked J107 (or J108). See Figure B-2.
2. Install the Interface Board in either of the two I/O slots in the Analyzer's Mother Board (see Figure B-1).
3. Install the cable attached to the board in the opening at J107 (or J108) on the Analyzer's rear panel.
4. Fasten the connector in place with the hardware supplied with the option.
5. Apply the supplied identifying decal to the rear panel connector location.

6. Dress the connector cable across the back of the boards and place any cable slack inside the Monitor compartment.
7. Remove the CPU Board from the Analyzer (see Figure B.1).
8. Locate the socket number marked on the chip (see Figure B-4 for location).
9. Install the chip in the correct CPU Board location.

When inserting a chip, take care to insert it firmly into the socket without bending any pins under the chip or leaving any pins outside of the socket. Be sure that the chip is plugged in with the notch in the chip toward the top of the board; the socket has a notch at the top as a guide.

CAUTION: Inserting the chip reversed will cause permanent damage to the chip when power is applied. Be certain that the chip is inserted correctly before replacing the board in the Analyzer.

10. Replace the CPU Board in the Analyzer.
11. Before replacing the Analyzer's covers, check the installation for proper operation.

B.14 MODEL 4272 GPIB INTERFACE

The Models 4271, 4272, 4273 are mutually incompatible. Only one of these may be in the Analyzer.

The GPIB Interface consists of the Interface Board, an identifying decal, a programmed integrated circuit (chip), and a ribbon cable. One end of the cable plugs into the board; the other end mounts on the Analyzer's rear panel.

The Model 4272 must be installed in a Series 40 which has Firmware version 2.3 or later. The Analyzer's Firmware version may be determined at power on (see Figure B.6)

If the Series 40's Firmware is version 2.2 or earlier, contact your local Canberra Representative or Canberra's Customer Service Department.

Before installing the Interface, be sure that the B0/B8 jumper is in the B0 position (refer to Figure B.14).

The eight switches in S1 (refer to Figure B.14) must be set before installing the board. Refer to Appendix B of the Model 4272 manual for a description of the switch functions.

To install the option:

1. Remove the CPU Board (see Figure B.1) and insert the supplied integrated circuit chip in socket A30 (see Figure B.4).

   When inserting the chip, take care to insert it firmly into the socket without bending any pins under the chip or leaving any pins outside the socket. Be sure that the chip is plugged in with the notch in the chip toward the top of the board; the socket has a notch at the top as a guide.

   CAUTION: Inserting the chip reversed will cause permanent damage to the chip when power is applied. Be certain that the chip is inserted correctly before replacing the board in the Analyzer.

2. Replace the CPU Board in the Analyzer.
3. Install the Interface Board in one of the Option Board slots (see Figure B.1).
4. Remove the cover plate from J107 on the rear panel. Compare J107 and J108. If J107 is larger than J108 you have a later version rear panel. Go on to step 12.
5. If J107 and J108 are the same size you have an earlier version rear panel. Go on to step 6.
6. Pass the small end of the ribbon cable through the opening and plug the cable into the Interface Board.
7. Pass the two screws removed with the cover plate through the opening's screw holes from the inside of the Analyzer.
8. Place the supplied lockwashers on the screws outside the rear panel.
9. Place the supplied standoffs on the screws and tighten the screws firmly into them.
10. Remove the nuts from the two supplied jackscrews and discard them.
11. Mount the ribbon-cable connector to the standoffs with the jackscrews. Tighten the jackscrews firmly and go on to step 17.
12. For later version rear panels, the standoffs are not needed; they may be discarded.
13. Remove the nuts from the two supplied jackscrews and mount the ribbon-cable connector on the J107 opening.
14. Pass the jackscrews through the mounting holes on the connector and through the opening's screw holes.
15. Place the two lockwashers on the jackscrews inside the rear panel.
16. Put the nuts on the jackscrews and tighten them down securely.
17. Fold about 5 cm (2 in.) of the ribbon cable down on the right side of the Interface Board. This will prevent the connector from pulling out of the board's socket.
18. Pass the rest of the cable to the left across the top of the other boards. Place any slack in the cable inside the Monitor Compartment.
19. Place the supplied identify decal on the rear panel connector.
20. Before replacing the covers, check the installation for proper operation.

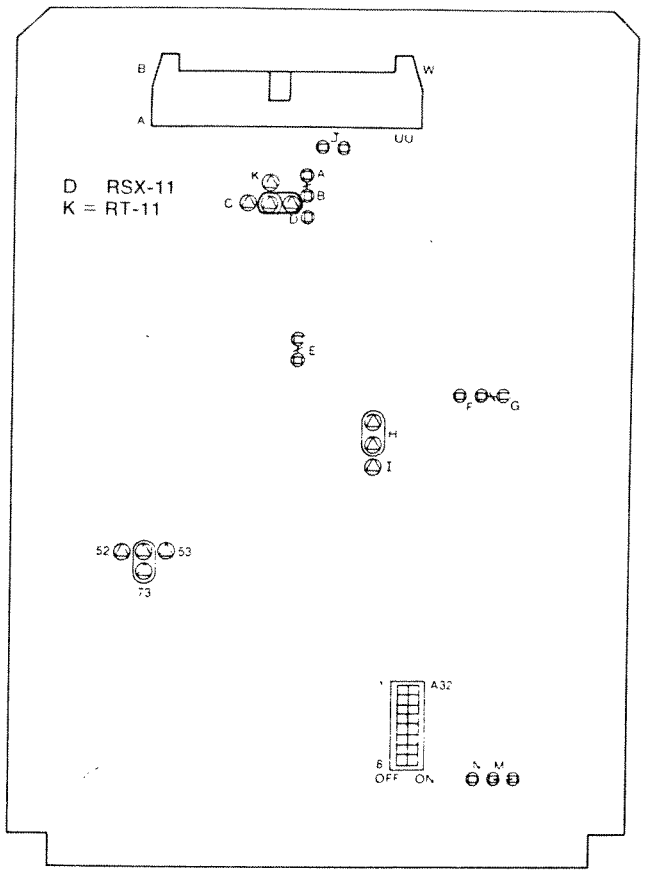


Figure B-13
Model 4271 Computer Interface Board

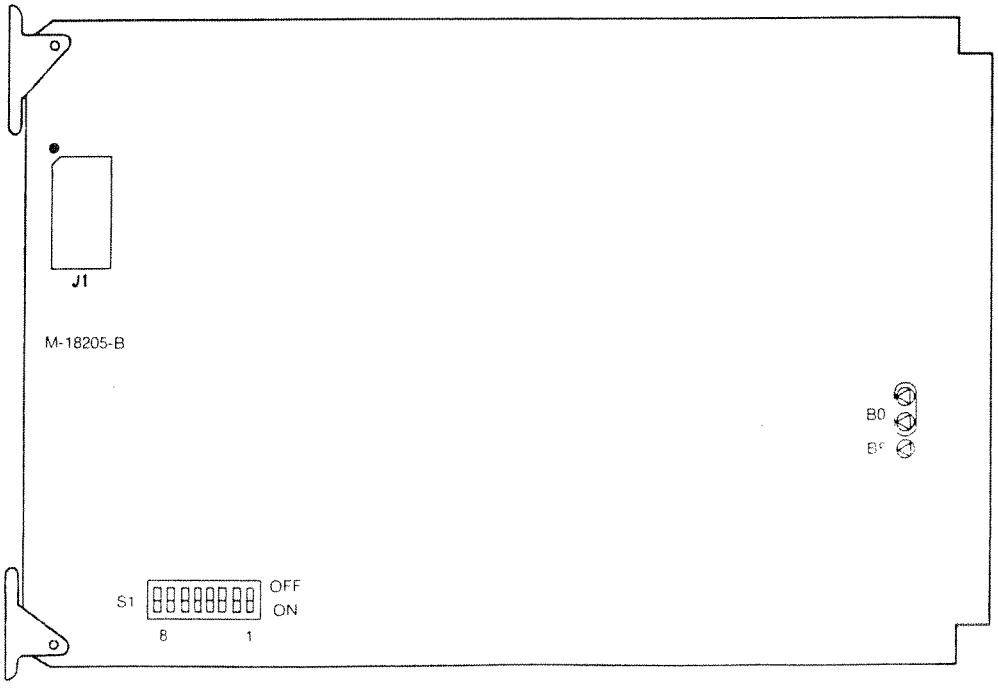


Figure B-14
Model 4272 GPIB Interface Board

B.15 MODELS 4273, 4273A, 4273B COMPUTER INTERFACES

The Model 4273 family of Computer Interfaces include: a printed circuit board with an attached cable, which is terminated in a 25-pin connector; two programmed integrated circuits (chips) marked with the Model number, the Firmware version number and a socket number; and an identifying decal. The Interface requires that the Model 4242 Learn/Execute option be installed in the Analyzer for proper operation.

Refer to the Model 4273 Operator's Manual for complete details on each of the Interfaces.

Refer to Section B-8 for Model 4242 installation instructions.

The Firmware version number on the chip must match the Firmware installed in the Analyzer. The Analyzer's Firmware version may be determined at power on (see Figure B-6).

If the two Firmware version numbers do not match, consult your local Canberra Representative or Canberra's Customer Service Department.

With Firmware version 2.1, the Models 4241 (Define/Use) and 4273 or 4273A are mutually exclusive - only one of the two may be installed in the Analyzer. With Firmware version 2.2 or later, both the Model 4241 and either the Model 4273/4273A or the Model 4273B may both be installed.

NOTE: The Model 4273/4273A and 4273B are mutually exclusive - only one of these can be operated at the same time by the Analyzer. The Model 4273B is not available for Firmware version 2.1.

Before installing the Interface Board in the Analyzer, check that the jumpers and switch positions are set correctly:

M-N jumper out (not used with Model 4273).
52/53/73 jumper in the 73 position
The remaining jumpers are used to configure the Interface Board to the user's needs; see the Model 4273 Operator's Manual, Appendix A, for jumper functions and switch settings.

To install the option:

1. Remove the rear panel plate which covers the opening marked J107 (or J108). See Figure B-2.
2. Install the Interface Board in either of the two I/O slots in the Analyzer's Mother Board (see Figure B-1).
3. Install the cable attached to the board in the opening at J107 (or J108) on the Analyzer's rear panel.
4. Fasten the connector in place with the hardware supplied with the option.
5. Apply the supplied identifying decal to the rear panel connector location.
6. Dress the connector cable across the back of the boards and place any cable slack inside the Monitor compartment.
7. Remove the CPU Board from the Analyzer.
8. Locate the socket number marked on the chip (see Figure B-4 for location).
9. Install the chips in the correct CPU Board locations.

When inserting a chip, take care to insert it firmly into the socket without bending any pins under the chip or leaving any pins outside of the socket. Be sure that the chip is plugged in with the notch in the chip toward the to of the board; the socket has a notch at the top as a guide.

CAUTION: Inserting the chip reversed will cause permanent damage to the chip when power is applied. Be certain that the chip is inserted correctly before replacing the board in the Analyzer.

NOTE: In Analyzers with version 2.1 Firmware, the Model 4273 uses one chip (A65); if there is a chip location A65 (the Model 4241 option chip), it will have to be removed before inserting the Model 4273 option chip. In Analyzers with later Firmware versions, the Model 4273 uses two chips; insert these chips in the socket location marked on each chip.

10. Replace the CPU Board in the Analyzer.
11. Before replacing the Analyzer's covers, check the installation for proper operation.

Appendix C
ADC Zero Adjustment Methods

C.1 ENERGY CALIBRATE METHOD

A basic method of adjusting the ZERO is outlined in the following steps:

1. Collect a spectrum and Energy Calibrate it (see section 5.13).
2. Make a note of the displayed energy equation.
3. Divide the equation's offset term by the energy per channel.
4. The result is the number of channels that the spectrum must be moved with the ZERO control so that zero energy falls in channel zero.
5. Clear the memory, disable ECAL, and adjust the ZERO so that the spectrum's peaks move that number of channels from their previous location. Repeatedly clearing the memory will aid in the correct placement of the peaks.
6. If the offset term displayed was a negative number, the spectrum must be moved leftward.
7. If the offset term displayed was a positive number, the spectrum must be moved to the right.
8. The ZERO should be readjusted each time the ADC GAIN is changed.

C.2 LIVE SOURCE METHOD

Alternatively, a live source with several peaks can be used for reasonable calibration accuracy. The source should have both high and low energy peaks, such as ^{57}Co and ^{60}Co.

1. The first step is to determine the energy per channel. For instance, 0.5 keV/channel for a 4096 ADC GAIN.
2. Adjust the amplifier's gain so that the high peak falls in its calculated channel. For ^{60}Co this would be channel 2665 (1332.5 keV divided by 0.5 keV/channel).
3. Adjust the ZERO so that the lower peak falls in its calculated channel. For ^{57}Co this would be channel 244 (122 keV divided by 0.5 keV/channel).
4. Repeat the high end adjustment using the amplifier's gain and the low end adjustment using the ZERO control until no further changes are seen.

The ADC is now properly adjusted for the ADC GAIN being used and the amplifier's gain may be changed as necessary without affecting the ZERO setting.

C.3 Pulser Method

The most accurate method uses Canberra's Model 8210 Precision Pulser, or equivalent.

1. Set the Series 40's MEMORY switch to:
   1/1 for the Model 4201 (displays 1024 channels)
   1/4 for the Model 4202 (displays 1024 channels)
   1/4 for the Model 4203 (displays 2048 channels)
2. Connect the Pulser to the ADC IN Connector with the ADC IN switch in the EXT position.
3. Set the Pulser's controls to HI, 0°, + and 0.5 μsec Rise Time.
4. The ADC GAIN and OFFSET as necessary for whichever baseline is to be determined:

GAIN	TOTAL OFFSET	OFFSET SWITCHES
8192	7168	1024, 2048, 4096
4096	3072	1024, 2048
2048	1024	1024
1024	none	none

NOTE: ADC Gains of 256 and 512 use the same ZERO setting as the 1024 Gain.

5. Set all of the binary switches on the Model 8210 to the ON (right-hand) position, turn the RELAY switch ON and adjust the COARSE and FINE AMPLITUDE controls so that the analyzer is collecting in channel 1023. It will be helpful to enable EXPAND to verify single-channel collection.
6. Set the Series 40's OFFSET to zero (all switches down) and set the upper six binary switches on the Model 8210 to OFF (the left-hand position).
7. Adjust the ZERO control on the Series 40 so that the analyzer is collecting in the proper channel as follows:

GAIN	CHANNEL
8192	127
4096	63
2048	31
1024	15

8. Repeat steps 4 through 7 until no further adjustments are necessary. In most cases, one repetition will be sufficient.
9. Note that the ZERO adjustment is made only for the one ADC GAIN setting being used. The ZERO need not be adjusted again unless another ADC GAIN is selected for use.

Appendix D
Computational Methods

1. Ratio computation:
   First data stored = the constant denominator
   Second data stored = a variable numerator
   Therefore, Ratio = $\frac{\text{data 2}}{\text{data 1}}$

2. Area computation:
   Area = Integral - (N/2) X (B_1 + B_2)
   where Integral = the total number of counts in the ROI
   N = v - u + 1 = the number of data channels in the ROI
   K = 4, the number of end points considered
   Xu = counts in u
   Xv = counts in v

   $B_1 = \frac{1}{a}\sum_{u}^{u+k-1} Xa$ k = estimated height of background on Left

   $B_2 = \frac{1}{a}\sum_{v-k+1}^{v} Xa$ k = estimated height of background on Right

   Background = (N/2) X (B_1 + B_2)

   Integral $= \sum_{a}^{v} Xa$

   AREA = Integral - Background

   This is shown graphically in Figure D.1, below:

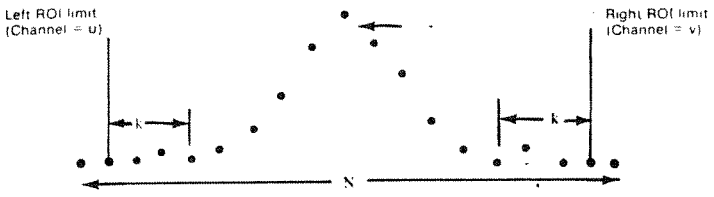


Figure D-1
Net Area

3. Stripping Computation:

   Y' = Y-FxX, where X and Y are two spectra in memory. The strip factor, F, may be a previously entered Factor, the last computed Ratio, or any other operator-specified value in the range:
   -327.675 < F < + 327.675

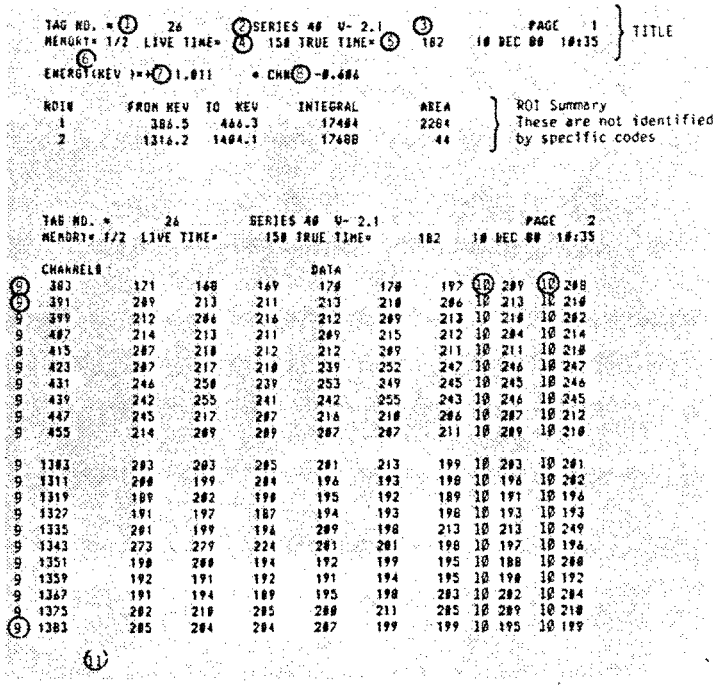
   The resultant spectrum (Y') replaces spectrum Y (the original spectrum); spectrum X is unchanged.

Appendix E
Input/Output Formats

E.1 SERIES 40 ASCII MODE OF I/O

ITEM	IDENTIFIER CODE (octal)	FIELD
1 TAGWORD	5	8 (ASCII) digits, leading spaces
2 HEADER ID	2	24 ASCII characters
3 TERMINATE HEADER and Variable length fields	3 (7 & 8)	
4 LIVE TIME or SWEEPS	36	8 (ASCII) digits, leading spaces
5 TRUE TIME or DWELL TIME	37	8 (ASCII) digits, leading spaces
6 UNITS	11	EV, KEV, MEV, MSEC, SEC, MIN
7 'B' coefficient	7	Floating Point FIELD (variable length terminated by Octal 3)
8 'C' coefficient	10	Floating Point FIELD (variable length terminated by Octal 3)
9 ACSII Address	33	5 digits, leading spaces
10 ASCII DATA	17	8 digits, leading spaces
11 END OF DATA (EOT)	4	Always used to terminate tape, in both ASCII and binary modes

Parity: in ASCII mode the eighth bit is parity for each character (byte).



TAG NO. = ① 26 ②SERIES 40 V- 2.1 ③ PAGE 1 } TITLE
MEMORY= 1/2 LIVE TIME= ④ 150 TRUE TIME= ⑤ 182 10 DEC 80 10:35 }
⑥
ENERGY(KEV)=+⑦1.011 * CHN⑧ -0.484

ROI#	FROM KEV	TO KEV	INTEGRAL	AREA
1	386.5	446.3	17484	2284
2	1316.2	1494.1	17488	44

} ROI Summary These are not identified by specific codes

TAG NO. = 26 SERIES 40 V- 2.1 PAGE 2
MEMORY= 1/2 LIVE TIME= 150 TRUE TIME= 182 10 DEC 80 10:35

CHANNELS	DATA								
⑨ 383	171	168	169	178	178	197	⑩ 209	⑪ 208	
⑨ 391	209	213	211	213	210	206	10 213	10 214	
9 399	212	206	216	212	209	213	10 210	10 202	
9 407	214	213	211	209	215	212	10 204	10 214	
9 415	207	210	212	212	209	211	10 211	10 210	
9 423	207	217	210	239	252	247	10 246	10 247	
9 431	246	250	239	253	249	245	10 245	10 246	
9 439	242	255	241	242	255	243	10 246	10 245	
9 447	245	217	207	216	210	206	10 207	10 212	
9 455	214	209	209	207	207	211	10 209	10 210	
9 1303	203	203	205	201	213	199	10 203	10 201	
9 1311	200	199	204	196	193	198	10 196	10 202	
9 1319	189	202	198	195	192	189	10 191	10 196	
9 1327	191	197	187	194	193	198	10 193	10 193	
9 1335	201	199	196	209	198	213	10 213	10 249	
9 1343	273	279	224	201	201	198	10 197	10 196	
9 1351	198	200	194	192	199	195	10 188	10 200	
9 1359	192	191	192	191	194	195	10 198	10 192	
9 1367	191	194	189	195	198	203	10 202	10 204	
9 1375	202	210	205	200	211	205	10 209	10 210	
⑨ 1383	205	204	204	207	199	199	10 195	10 199	

⑫

Figure E-1
Sample ROI Readout from Series 40
ASCII Mode

Each line ends with: CR NU NU NU NU LF

E.2 SERIES 40 BINARY MODE OF I/O

The memory data is transferred in a binary format. Each Region to be transferred is organized into a Data Block with the following characteristic:

Identifier Code $(34)_8$

Region Channel Count Low Byte Region Channel Count High Byte	(n)
Starting Channel Address Low Byte Starting Channel Address High Byte	
Data High Byte Data from Starting Data Low Byte Address Data Middle Byte	(1)
Data High Byte Data from last Data Low Byte channel in region Data Middle Byte	(n)

The tape output will be:

Title and Header as in ASCII mode
Data Block 1
Data Block m
EOT $(4)_8$

Parity: In Binary mode, no parity is maintained.

Appendix F
Ap-Pak Equations

Note: In all equations, ROI #0 means the current ROI; that is, the ROI where the cursor is currently located or the next ROI to its right if the cursor is not in an ROI.

Equation Number	Name	Definition
5	Peak Centroid	V1, where V1 = centroid @ ROI #0.
6	Peak FWHM	V1, where V1 = FWHM @ ROI #0.

The Centroid routine finds the highest data point in the current ROI after correcting for a four-point averaged background.

The FWHM routine subtracts the background from the centroid peak-count and divides by 2, then finds the channel on the left side equal to or less than the half-count, background corrected. The FWHM is the number of channels between those two points.

7	Counts/Second	V1/TL, where V1 =0
8	Percent Error	165 * (SQRT(V1))/V1, where 165 = 90% confidence and V1 = AREA @ ROI #0.
9	Percent Dead Time	((V1-TL)V1 * 100 where V1 = CNT @ CH #1.
10	Half Life	K1, where K1 = the half life for EQUA #11 and EQUA #13.
11	Efficiency	(V1/TL)/(K1 * EXP(-0.693 * K2/V2)), where K1 = Gammas/sec, K2 = Decay time in same time units as EQUA #10, V1 = AREA @ ROI #0, and V2 = EQUA #10.
12	Activity in μCi	(V1/TL)/(3.7E4 * V2 * K1) where K1 = Gammas per disintegration, V1 = AREA @ ROI #0, and V2 = EQUA #11.
13	Decay Corrected Activity	V1/EXP(00.693 * K1/V2), where K1 = Decay time in same time units as EQUA #10, V1 = EQUA #12, and V2 = EQUA #10.
14	Dose Rate mR/hr	(0.5 * K1 * V1 * V2)/(K2 * K2), where K1 = Yield (Gammas/disintegration), K2 = Detector-to-source distance in meters, V1 = EQUA #5 and V2 = EQUA #12.

Appendix G.
Firmware/Option Compatibility

This chart shows the compatibility of the Series 40's options with successive versions of the Firmware.

The left-hand column lists the Basic Set of the Series 40's Firmware and all available options. Each suceeding column lists each version of the Firmware, showing which chip numbers are installed on the CPU Board for the Basic Set and for each option.

Note that some options (for instance, RECYCLE) use one of two possible chip types (2716 or 2732). The 2716 type is used with Firmware version 2.2 and later. The 2732 type is used with Firmware version 2.1.

For version 2.1, each chip is labeled with the CPU Board socket number. For version 2.2 and later, each chip is labeled with the socket number, the Firmware version number and either '-00", indicating that this chip is part of the Basic Firmware set, or "-n", where "n" is the option number.

Version	V2.1	V2.2	V2.3	V2.4
4201,4202, 4203 Basic (2732)	YES A50, A51, A52, A53, A64, A66	YES A50, A51, A52, A53, A64, A66-2.2-00	YES A50,A51,A52, A53, A64, A66-2.3-00	YES A50, A51, A52 A53, A64, A65, A66-2.4-00
RECYCLE[3]	YES	YES	YES	YES
(2716)	N/A	A14-2.2-00	A14-2.3-00	A14-2.4-00
(2732)	A67	N/A	N/A	N/A
4221	YES	YES	YES	YES
4222	YES	YES	YES	YES
4223	NO	YES	YES	YES
4231	YES	YES	YES	YES
4231A	NO	NO	NO	YES
4232	YES	YES	YES	YES
4233	YES	YES	YES	YES
4241	YES[1]	YES	YES	YES[9]
(2716)	N/A	A12, A13,,-2.2-41	A12, A13-2.3-41	A12, A13, A29-2.4-41
(2732)	A65	N/A	N/A	N/A
4242[3]	YES	YES	YES	YES
(2716)	N/A	A14, A15-2.2-42	A14, A15-2.3-42	A14, A15-2.4-42
(2732)	A67	N/A	N/A	N/A
4251	YES[2]	YES	YES[5]	YES[5]
(2716)	N/A	A29-2.2-5.1	A28-2.3-51	A28-2.4-51
(2732)	A53	N/A	N/A	N/A
4252	NO	NO	YES[5]	YES[5]
(2716)	N/A	N/A	A28-2.3-52	A28-2.4-52
4253	YES[2]	YES	YES[5]	YES[5, 10]
(2716)	N/A	A28-2.2-53	A28-2.3-53	A28-2.4-53
(2732)	A53	N/A	N/A	N/A
4254	NO	NO	YES[6]	YES[6, 9]
(2716)	N/A	N/A	A29-2.3-54	A29-2.4-54
4271	NO	NO	YES[7]	YES[7]
(2716)	N/A	N/A	A30, A31-2.3-71	A30, A31-2.4-71
4272	NO	NO	YES[7]	YES[7]
(2716)	N/A	N/A	A30-2.3-72	A30-2.4-72
4273/4273A	YES[1]	YES[4]	YES[7]	YES[7]
(2716)	N/A	A30, A31-2.2-73/A	A30, A31-2.3-73/A	A30, A31-2.4-73/A
(2732)	A65	N/A	N/A	N/A
4273B	NO	YES[4]	YES[7]	YES[7]
(2716)	N/A	A30, A31-2.2-73B	A30, A31-2.3-73B	A30, A31-2.4-73B
4274	NO	NO	YES[6, 7, 8]	YES[6 7]
(2716)	N/A	N/A	A30-2.3-74	A30-2.4-74

FOOTNOTES:

[1]In V2.1 4241 and 4273/4273A are mutually exclusive.
[2]In V2.1 4251 and 4253 are mutually exclusive.
[3]In all versions 4242 and Recycle are mutually exclusive.
[4]In V2.2 4273/4273A and 4273B are mutually exclusive.
[5]In V2.3 and subsequent 4251, 4252, 4253 are mutually exclusive.
[6]AR #11316 required for 4254 and 4274. 4254 and 4274 are mutually exclusive.
[7]In V2.3 and subsequent 4271, 4272, 4273/4273A, 4273B and 4274 are mutually exclusive.
[8]In V2.3 4274 is available on Special Order only.
[9]4241 and 4254 in same box require Special Order.
[10]Requires Revision D or subsequent of Interface Board.

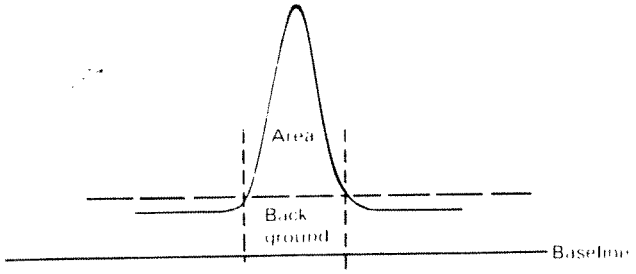
Revision D or subsequent of CPU Board is required for all versions of firmware. (Previous revisions will not support 2732 EPROM's).
Revision D or subsequent of Mother Board is required for Option 4223, 4254, and 4274.
AR #11,154 for Display Board is required for V2.2 and subsequent on 4203 (may be used for 4201 and 4202).

GLOSSARY OF TERMS

ADC—Analog to Digital Converter. An electronic instrument which generates a digital word representing the magnitude of an analog signal.

ANTICOINCIDENCE GATING—The use of a logic pulse to trigger the rejection of a signal pulse by a signal processing device.

AREA—The number of counts in a given region that are above a determined background level. Equal to the region's integral minus the background.



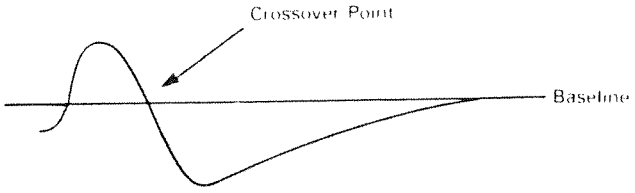
Area = Integral − Background

ASCII—American Standard Code for Information Interchange. A standard method of encoding alphabetical and numerical characters for digital transmission.

BASELINE—A reference from which a pulse excursion varies. Usually zero volts.

BASELINE, ADC—See ZERO, ADC.

BIPOLAR PULSE—A pulse that has successive excursions in both the positive direction and the negative direction from the baseline.



BNC—A type of coaxial cable connector.

CHANNEL—An MCA memory location used to store one word of spectral data.

COINCIDENCE GATING—The use of a logic pulse to trigger the acceptance of a signal pulse by a signal processing device.

COLLECT—An MCA function that causes storage of data in memory.

COUNT RATE STABILITY—The degree to which the amplitude of a pulse is distorted by variations in the average pulse rate.

CONVERSION GAIN, ADC—The number of discrete voltage levels that the ADC's full scale input is divided into. Commonly a binary multiple of 256 channels.

CONVERSION TIME—The time required to change an input signal from one format to another, such as analog to digital; contributes to Dead Time.

CROSSOVER TIME—The time at which the bipolar pulse passes through a designated level; usually the baseline. See BIPOLAR illustration.

CRT—Cathode Ray Tube. A visual display device similar to a television receiver picture tube.

CURRENT LOOP—A continuous current path, usually carrying 20 milliamperes, between the sending unit and the printer.

CURSOR—A vertical marker in the MCA display. Can be moved to a channel or area of interest; the display shows cursor location and channel count as numeric data.

DEAD TIME—The time that the processing circuits are busy processing a signal and are not able to accept another pulse. Often expressed as a percentage.

DECAY TIME—The time interval during which a pulse drops from its original peak amplitude to a stated fraction of its original amplitude.

DIFFERENTIAL NONLINEARITY—Maximum channel to channel deviation from the ideal uniformity of channel width. The measure of how nearly all channels have the same incremental voltage width.

DWELL TIME—The sampling interval per channel in the Multichannel Scaling mode of data acquisition.

EIA RS232C/RS422—(United States) Electronic Industries Association standards for transmitting digital information.

ENERGY CALIBRATION—An MCA function where the displayed energy spectrum is calibrated for a specific unit of energy per channel. Allows unknown energy peaks to be identified by their location in the calibrated spectrum.

EXPAND—An MCA function where a specific ROI is expanded to the full width of the display screen for close examination.

FALL TIME CONSTANT—The time required for a pulse to fall from its original peak amplitude to 37% of its original peak amplitude.

FWHM—Full Width at Half Maximum. The full width of a distribution measured at half of the maximum amplitude. Defines spectrum resolution.

GAIN—The ratio of the amplifier's output signal to its input signal.

GPIB—General Purpose Interface Bus. Equivalent to the Hewlett-Packard Interface Bus (HPIB). Complies with IEEE-488 specifications.

GAUSSIAN PULSE SHAPE—A pulse shape resembling a statistical bell-curve and having little or no overshoot or ringing. See UNIPOLAR PULSE illustration.

HISTOGRAM—A representation of an energy peak by means of vertical bars, the heights of which indicate the frequency of the energy events.

IMPEDANCE MATCHING—The necessity of terminating a signal line in its characteristic impedance (listed in the product specifications) to allow optimum transfer of undistorted signals from one device to another.

INPUT/OUTPUT—The process of introducing data into or extracting data from an MCA using a peripheral recording device, such as a Teletype or a Cassette Tape.

INDEX—An MCA function that jumps the cursor(s) from one ROI to another.

INTEGRAL (MCA)—The sum of the absolute number of counts in all channels in a given region. See AREA illustration.

INTEGRAL NONLINEARITY—The measure of the deviation of a signal from a theoretical straight line between zero and its maximum value, expressed as a percentage of the full scale value.

INTENSIFY—A brighter region of the display which visually sets a Region of Interest off from data regions of lesser importance.

I/O—See INPUT/OUTPUT.

LINEARITY—Invariance (within specified limits) of amplitude and/or timing of an output with reference to the same input repeated over a significant period of time.

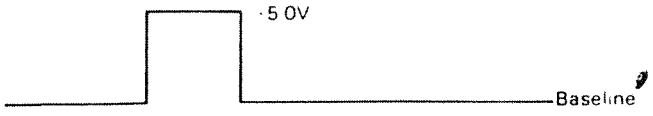
LIST—A data acquisition mode where each converted input is stored sequentially, one conversion per channel.

LIVE TIME—The time that the processing circuits are not busy processing a signal.

LIVETIME CORRECTION—The process of stopping the Live Time clock in the MCA whenever the processing circuits are busy and can accept no further information. Commonly used to extend the collection time by accounting for the Dead Time.

LLD—Lower Level Discriminator - a comparator that outputs a logic pulse when the analog input exceeds a preset reference voltage level.

LOGIC PULSE—Generally refers to a TTL compatible logic pulse: 2.5 to 5.0 volts is a high level; less than 0.5 volts is a low level. Width is defined by use.



MCA—MultiChannel Analyzer.

MCS—MultiChannel Scaling. Distribution of events versus time.

MEMORY—An electronic device which acts as a data storage medium.

MIXER/ROUTER—An electronic instrument that accepts several inputs and routes each into a separate section of the MCA memory.

NIM—Nuclear Instrumentation Module.

NOISE—Unwanted disturbances on or with a useful signal which tend to obscure its information content.

NORMALIZE—An MCA function where data in a given area or in the whole memory is adjusted by addition of and/or multiplication by operator specified factors. Used to adjust the data so that it falls within a prescribed range.

OFFSET, ADC—A digitally performed shift in the zero channel of the ADC. Shifts the entire spectrum by the selected number of channels.

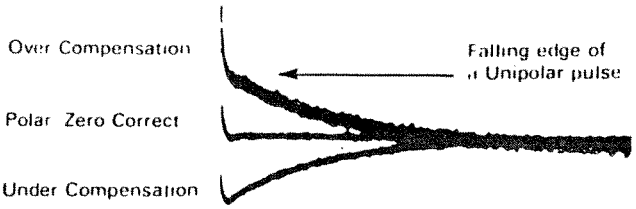
OVERLAP—An MCA function where a section of memory can be displayed with a reference section. Usually offset by some percentage of the reference section.

PEAK—A statistical distribution of digitized energy data for a single radioisotope.

PEAK CHANNEL—The channel number corresponding to the peak of a radioisotope's energy distribution.

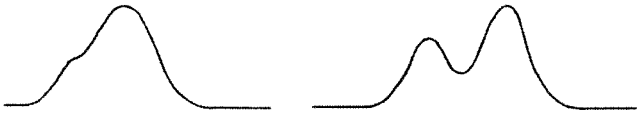
PHA—Pulse Height Analysis. Distribution of event amplitudes versus frequency of event occurrences.

POLE/ZERO—A method of compensating the Preamplifier's output signal fall time and the Amplifier's shaping time constant. Its use improves the Amplifier's high count rate resolution and overload recovery.



PULSE PAIR RESOLUTION—The ability to discriminate between two pulses close together in time.

PULSE PILEUP—A condition where two succeeding pulses are so close together in time that the beginning of the second pulse occurs before the first pulse has returned to the baseline, thus giving the second pulse the appearance of a greater pulse height than it actually possesses.



Leading Edge Pileup Trailing Edge Pileup

PULSE PILEUP REJECTOR—An electronic circuit for sensing the pileup condition and rejecting the piled up (convoluted) pulses from processing.

RANGE, ADC—The full scale address of the ADC memory group.

REGION OF INTEREST—A user-determined area of the MCA display which contains data of particular interest, such as a Peak.

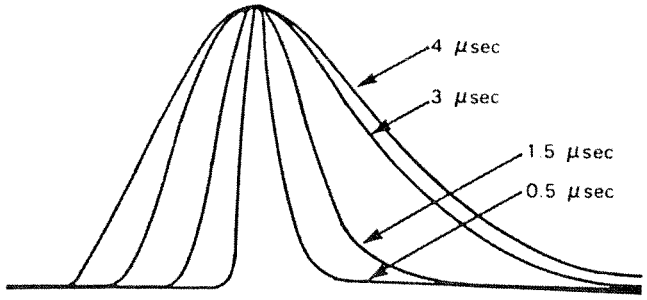
RESOLUTION—The ability of an amplifier or a detector to differentiate between two peaks that are close together in energy. Thus, the narrower the peak, the better the resolution capability. Measured as FWHM.

RESTORER (BASELINE RESTORATION)—A circuit usually used at the spectroscopy amplifier output to define a dc reference baseline (normally 0 volts).

ROI—See Region of Interest.

SCA—Single Channel Analyzer - recognizes events (pulses) that fall within two voltage limits (an LLD and a ULD) set by the operator. Outputs a logic pulse for each event recognized.

SHAPING—A process of modifying the input pulse shape to one more suitable for ADC processing.



SHV—Safe High Voltage connector.

SLOW NIM SIGNAL—See Logic Pulse.

SMOOTH—An MCA function where the data in one channel is averaged with data in adjacent channels in order to decrease or eliminate random data fluctuations.

SPECTRUM—A distribution of radiation intensity as a function of energy or time.

SPECTRUM BROADENING—A figure of merit indicative of overall system performance. Influenced by imperfections in the detection system, including detector ballistic deficit, system (electronic) noise and pulse pile-up.

STRIP—An MCA function where an operator specified fractional part of the data in one section of memory is subtracted from the data in another section of memory. The data in the first section remain unchanged.

SYSTEM BUSY TIME—The Dead Time of an entire Spectroscopy System.

TERMINATOR—A load at the terminal end of a signal line.

THROUGHPUT—The capability of processing data in a specified time (n bits or pulses per second, for instance)

TIME TO PEAK—The time taken by a signal pulse to go from a specified level near the baseline (point of origin) to the pulse peak. See UNIPOLAR PULSE illustration.

TRANSFER—An MCA function where data in one section of memory can be copied into another section of memory without clearing data from the first section.

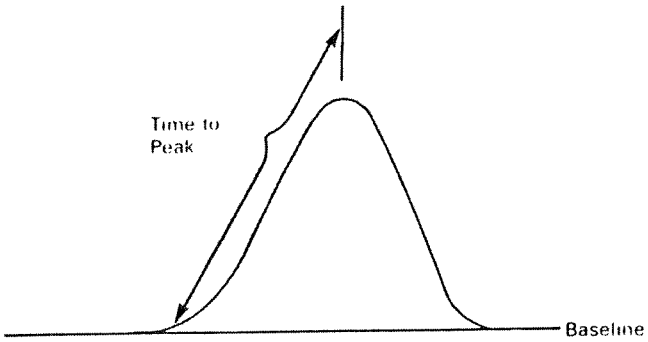
TRIGGER—A signal, usually a pulse, which initiates action in a circuit.

TRUE TIME—Real clock time.

TTL PULSE—See Logic Pulse.

ULD—Upper Level Discriminator - see LLD.

UNIPOLAR PULSE—A pulse that has an excursion in only one direction (either positive or negative) from the baseline.

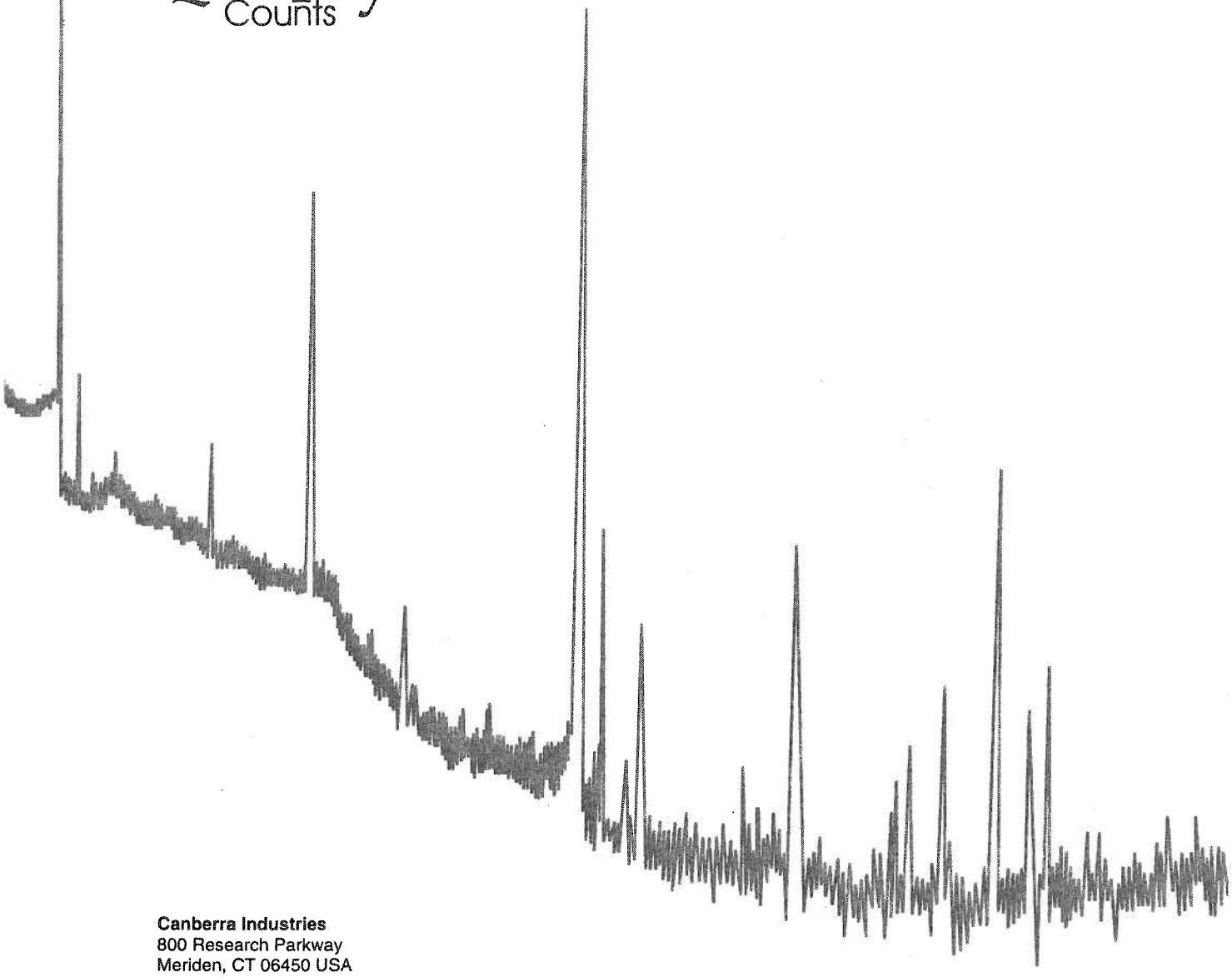


WINDOW (MCA)—The MCA EXPAND function's ability to move through the displayed spectrum while retaining its original width (number of channels).

ZERO, ADC—The zero energy channel of the ADC, which is commmonly aligned with channel zero of the memory. See OFFSET, ADC.

CANBERRA

Where Quality Counts



Canberra Industries
800 Research Parkway
Meriden, CT 06450 USA
Tel: 203-238-2351
FAX: 203-235-1347
Internet: http://www.canberra.com

Canberra-Packard Pty. Ltd.
Mt. Waverley, Victoria, Australia

Canberra-Packard Ges.m.b.H.
Vienna, Austria

Canberra-Packard Benelux NV-SA
Zellik, Belgium

Canberra Semiconductor N.V.
Olen, Belgium

Canberra-Packard
Greve, Denmark

Canberra-Packard Ltd.
Pangbourne, Berkshire, England

Canberra Electronique SA
Savigny-le-Temple Cedex, France

Canberra-Packard GmbH
Dreieich, Germany

Canberra-Packard Trading Corporation
Moscow, Russia